WESTINGHOUSE ELECTRIC CORPORATION
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FINAL REPORT

CONTRACT NAS8-11899

Design, Develop, Fabricate and Deliver
20-Watt Integrated Oscillator Amplifiers

Covering Period April 15, 1965
to August 15, 1966

National Aeronautics and Space Administration
G.C. Marshall Space Flight Center
Huntsville, Alabama 35812

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I. INTRODUCTION

A. REVIEW OF SPECIFICATIONS

The initial design objective of this contract was to produce a 70-watt oscillator with the following properties (taken from the original proposal):

1. General Requirements

Physical size to be as small as possible to meet the electrical and reliability requirements. Preferably the device shall be fabricated in a single stud mounted package containing a single silicon slice. If this does not seem feasible due to thermal considerations, a single package containing two silicon chips or two packages each containing a single silicon chip will be considered.

2. Mechanical Specifications

a. Device shall be hermetically sealed

b. Device shall be electrically isolated from the case.

3. Electrical Specifications

a. Suggested circuit configuration of the device is included as Figure 1.

b. Utilization as oscillator is shown in Figure 2.

c. Utilization as a switching amplifier is shown in Figure 3.

d. The available supply voltage is 25 to 30V dc.

e. The maximum collector current shall be 3 amps.

f. The minimum current gain of the transistors shall be 30 at the saturation current of 3 amps over the temperature range of -55°C to 125°C.

g. The drop from collector to emitter for 3-amp collector current shall be less than 1 volt.

h. A minimum V_{CEO} sustaining voltage of 100V is required. A higher value would be preferable if possible.

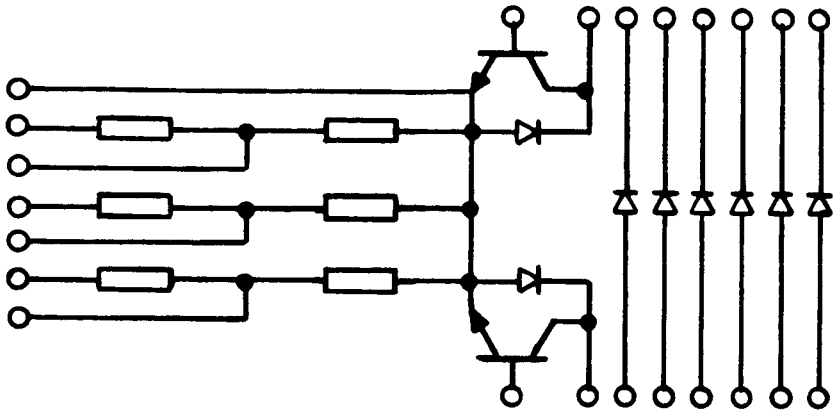


Figure 1: Suggested Circuit Configuration

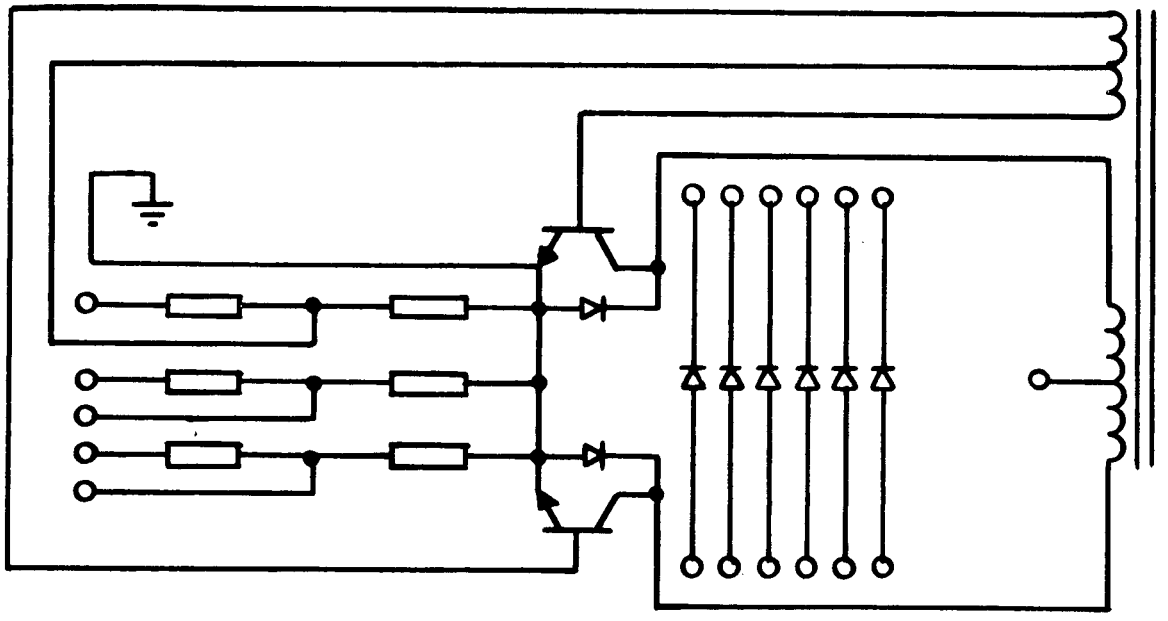


Figure 2: Proposed Device as Oscillator

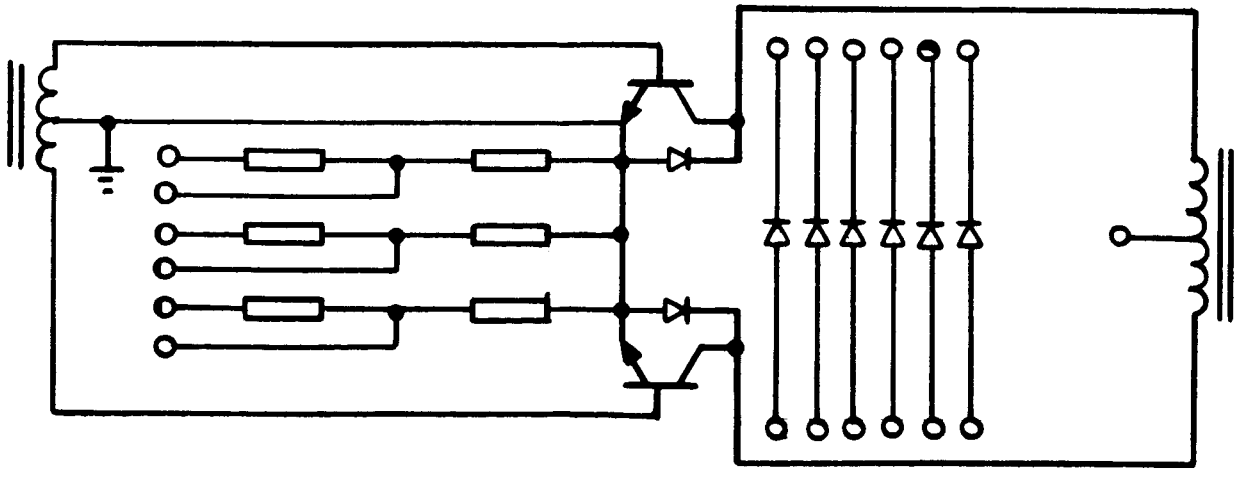


Figure 3: Proposed Device as Switching Amplifier

i. The back-up diodes should be adequate to protect the transistors when operating with inductive loads.

j. The auxiliary diodes should be quite versatile. They should be capable of carrying 10A under a 50% duty cycle. The drop across the diode should not exceed 1V when carrying 10A. The voltage rating should be in excess of 200V.

k. When operating as an oscillator (Figure 2), a choice of R_1, R_2, R_3, R_4 or R_5 shall be available for different levels of operation.

l. The oscillator/amplifier should be capable of 20kc operation without appreciably distorting a rectangular wave. The rise time of the output for a step input and current gain of 30 shall be less than 1 microsecond.

4. Environmental Specifications

a. Temperature Cycling: -55°C to 200°C, 5 cycles

b. Moisture Resistance: 10 cycles

c. Centrifugal: 500g

d. Shock: 500g

e. Vibration: 20g, 100cps to 2000cps

NOTE: After acceptance inspection of the units furnished by the Contractor, MSFC may elect to subject the unit to operation during and after nuclear radiation exposure. Exposure will be 1×10^{13} NVT ($E > .5$MeV) and 5×10^5 R. Maximum exposure rates will be 1.8×10^5 R/HR and 7×10^{13} neutron/cm^2/hr. The contractor will be notified of this test and invited to have a representative witness such a test.

In order to clarify our approach, interpretation as follows has been placed on the indicated item:

Item 2a - "Hermetically Sealed" is taken to mean that the encapsulation will have a leak rate no greater than 1×10^{-5} std cc/min. as determined by a helium mass spectrograph.

Item 3f - Temperatures are assumed to be case temperature as measured on the periphery of the copper pedestal above the stud.

Item j - Voltage and current values are assumed to be peak values.

Item 3k - It is assumed the last set of resistance combination refers to R_5, R_6. The choice of R value shall be maintained within practical limits of the suggested process.

During the contract period the objective was changed from a 70-watt oscillator to a 20-watt oscillator. Three 70-watt prototypes and ten 20-watt final samples were to be fabricated. The switching capability was to be raised from 20kc to 50kc and the package size was to be reduced.

B. MAJOR DIFFICULTIES ENCOUNTERED

Three prototype samples of the 70-watt oscillator were fabricated and encapsulated in a single stud mounted package. Difficulties were encountered in obtaining satisfactory packages for the 20-watt version. The initial supplier did not meet delivery dates and when the packages were received they were unsatisfactory. A new 16 lead flat pack from Coors (Coors' package #A-1212-88-CS) was evaluated and found to be satisfactory. The difficulties in obtaining packages delayed the evaluation of the oscillator in the breadboard circuit. Had this evaluation been accomplished earlier, there might have been time to evaluate some of the suggestions discussed in the Conclusions and Recommendations section.

High $V_{CE(sat)}$ values were a problem with the 70-watt version. The 20-watt version has satisfactory values of $V_{CE(sat)}$. The transistor gain is lower than is desirable. Initial calculations indicated a P diffusion of 150 Ω-cm and 5μ X_j would serve for both the base and resistor diffusions. Circuit analysis indicates that gains of 100 or greater are desirable for efficient operation.

Had this been known earlier, separate diffusions for the base and resistors would have been employed.

Scribing and breaking was used to separate the units from the wafer. This initially caused very low yields because: 1) scribing across the deep isolation grooves between transistors is difficult, and 2) the wafers have

a tendency to break at the etch groove during the breaking step. Initial experiments on Run SM-1 yielded only one complete unit from 24 possible ones. Different types of diamond scribing tools were evaluated.

The optimum tool is a commercially available phono point diamond scribe with a 3-mil radius. It is a truncated crystal with an easily determined orientation vector. A 20-gram weight gives the best results. After scribing, the wafer is broken between two sheets of plastic to minimize damage to the metallized areas. This is necessary because with the tight tolerances of the 20-watt unit any smearing of the Al would cause electrical shorts. With these improved techniques later runs were diced with good definition and with yields approaching 100%.

C. MAJOR ACCOMPLISHMENTS

Three 70-watt oscillators and ten 20-watt oscillators were fabricated and encapsulated. For the 20-watt version the package size was reduced and the switching raised from 20KC to 50KC. Efficiencies of greater than 90% have been observed, demonstrating the feasibility of integrating power devices.

II. DESIGN CONSIDERATIONS

Figure 4 is a detailed drawing of the 70-watt oscillator. Three prototype samples using this geometry were fabricated. All the oscillator components are on a single Si chip. The Si chip is 370-mils square. Each transistor has a emitter edge length of 900 mils. There are three resistor networks which, for a sheet resistivity 125 to 150 ohms per square, make possible a selection of resistors up to 7000 ohms.

Figure 5 is a detailed drawing of the 20-watt monolithic oscillator. The ten final samples were fabricated using this geometry. The Si chip size is 320 mils by 200 mils. Each transistor has an emitter edge length of 210 mils. There are six resistor taps. The 7500 ohms and 500 ohms can be obtained with a diffusion of from 125 to 150 ohms per square. The higher valued resistors necessary for 8-watt operation are impractical because they would occupy too much space.

Process details are discussed in a later section. As mentioned previously, the base and resistors are formed during the same diffusion operation. Recent design analysis, based on circuit test results, indicate that it would be necessary to perform a separate base and a separate resistor diffusion to obtain transistors with a high gain and resistors with the desired values.

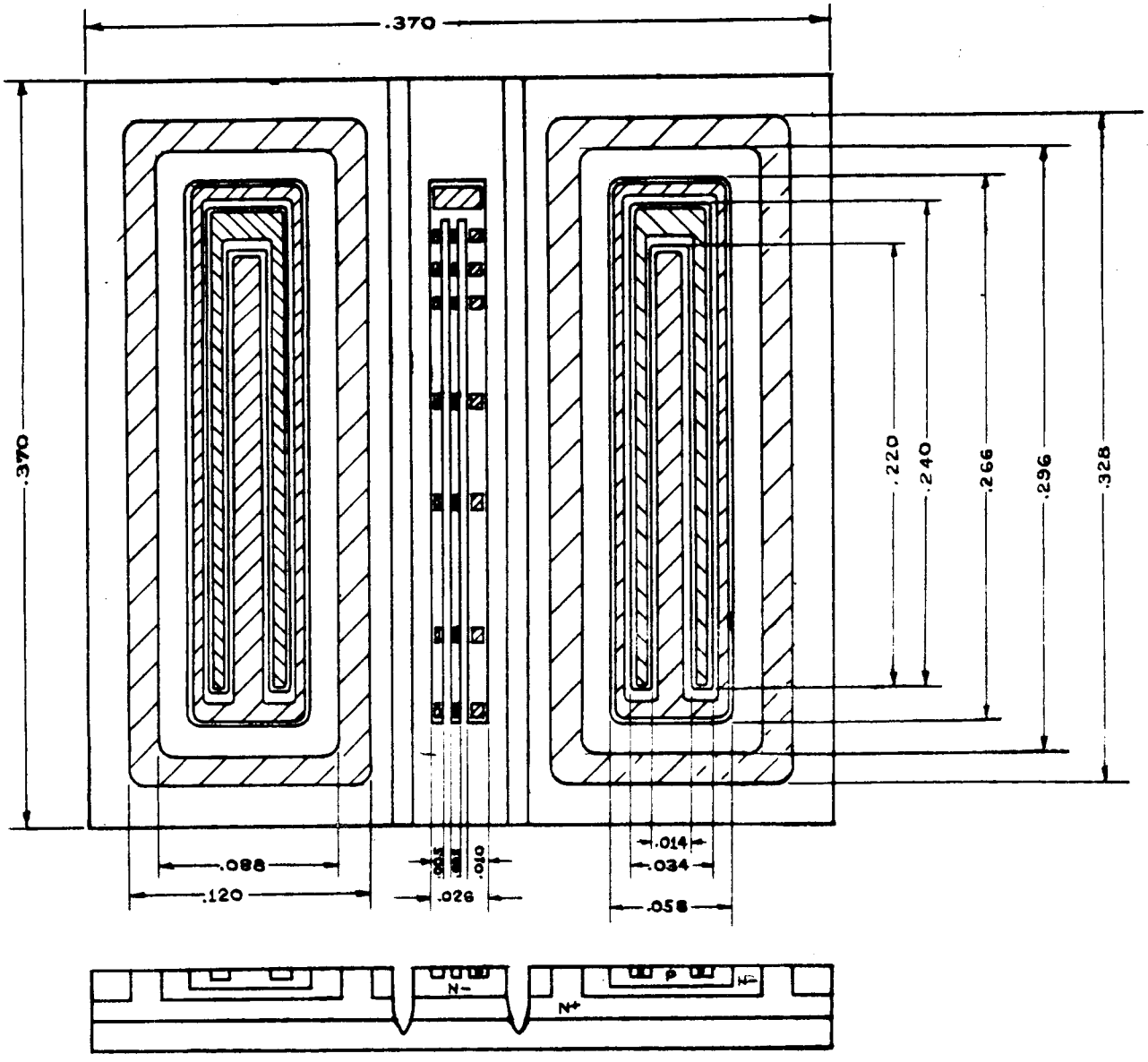


Figure 4: 70-Watt Oscillator

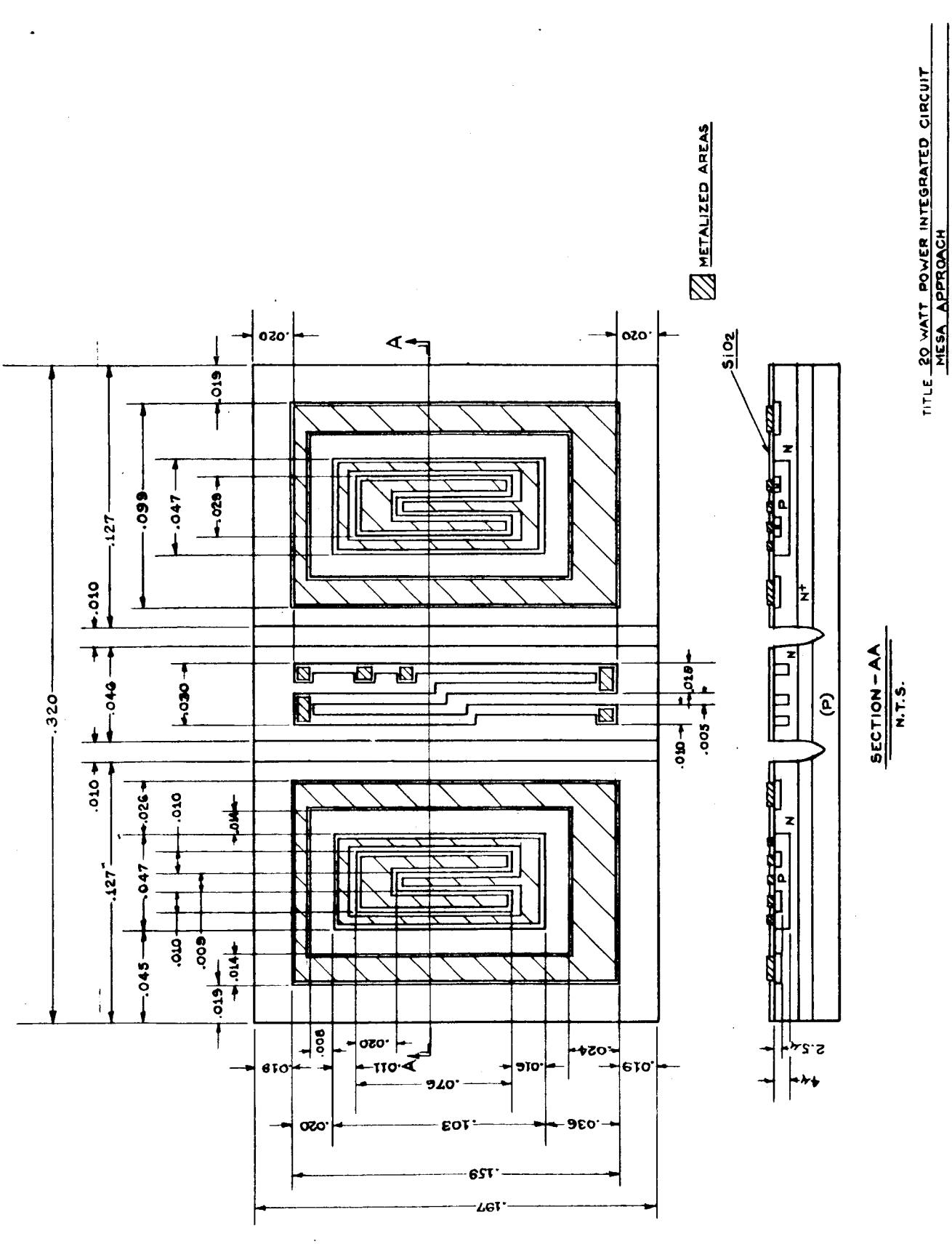


Figure 5: 20-watt Oscillator

III. DEVICE FABRICATION

Figure 6 is a process flow chart for the mesa version of the 20-watt oscillator. Continued reference to this figure will make the process details which follow easier to understand.

A. EVALUATION AND PREPARATION OF MATERIAL

1. Conductivity

This measurement determines the majority carriers in the silicon crystal. Two methods are employed at this laboratory - thermoelectric cold probe method (see Figure 7) and the point contact rectifier method.

2. Resisitivity

The resistivity is measured every inch down the length of each crystal to insure the accuracy of reading supplied by the supplier. A Fell's four-point probe is utilized for this operation; a probe spacing of 0.025" is used.

3. Radial Resistivity Gradient

This measurement is made on a silicon slice using a 0.025" Fell's four-point probe. Readings are made in the center and at 1/2 radius, and the gradient calculated from the data obtained. This is to insure a uniform distribution of dopant atoms in the slice.

4. Diameter

This material is centerless ground by the supplier to our specification. Buying the material to size eliminates the necessity of cavitroning, etching, or sandblasting.

5. Dislocation Density

This parameter is checked on both the seed and the end of the crystal opposite the seed. These slices are etched in chromium trioxide to reveal the etch pits, and a count is then made to determine the number/cm^2.

20 WATT OSCILLATOR
PROCESS FLOW CHART

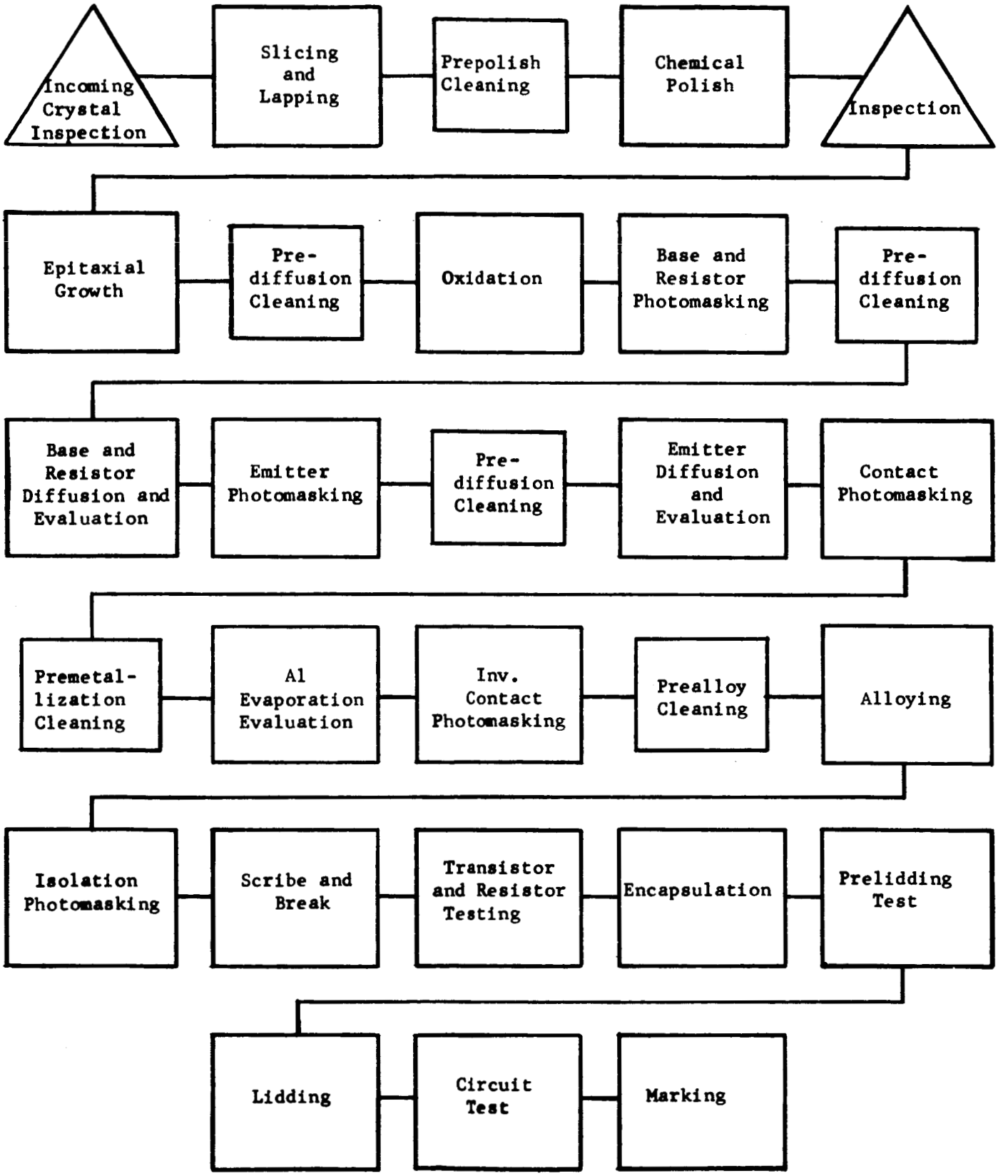
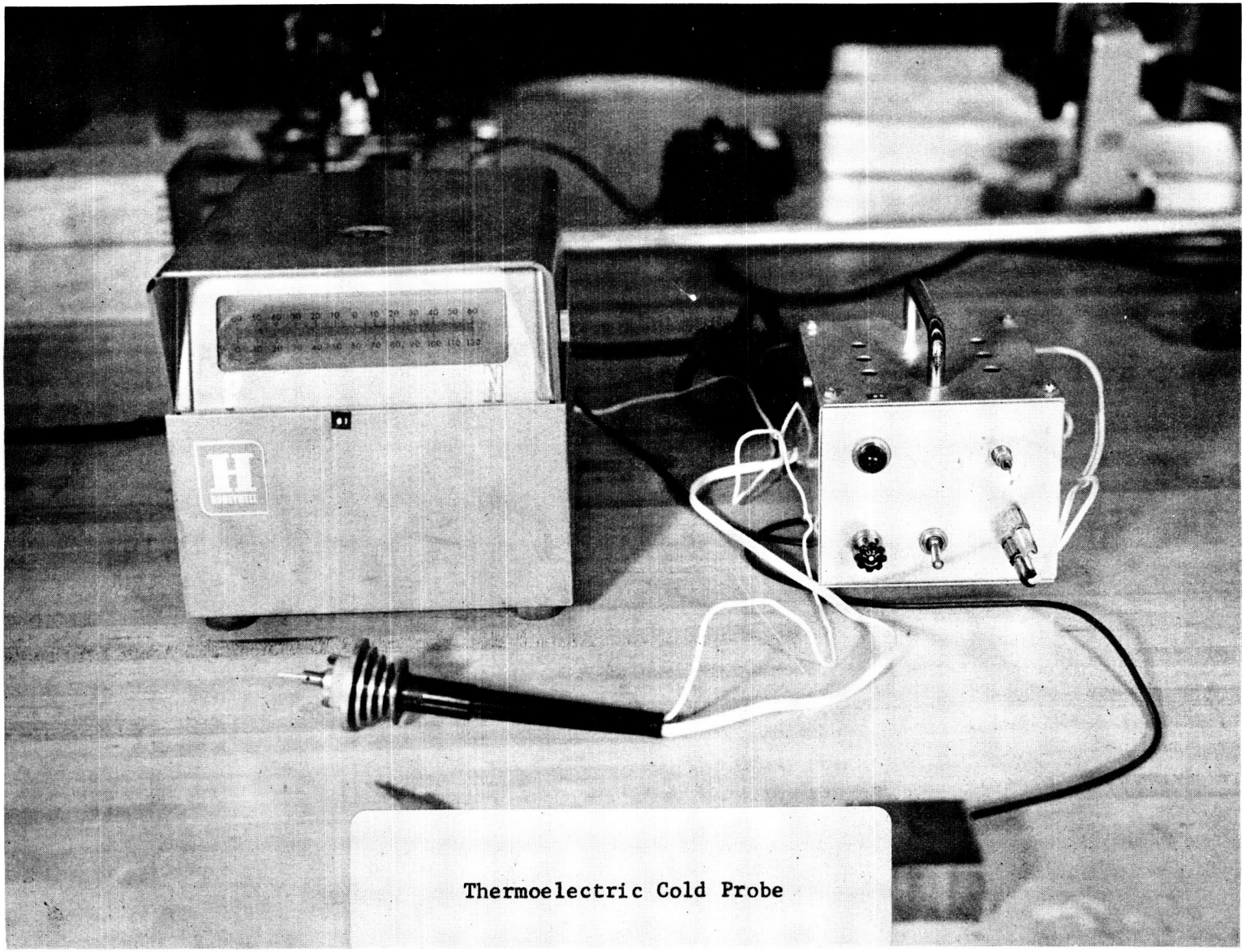


Figure 6: Process Flow Chart



Thermoelectric Cold Probe

Figure 7

6. Orientation

A photograph of the orientation apparatus is shown in Figure 8. The primary objective is to insure that after sawing there will be a round slice at 0° on the (111).

7. Lifetime

The lifetime equipment is illustrated in Figure 9, which is a photoconductive decay instrument. The crystal is first degreased, washed with pure water and dried, the ends of the crystal are then gold plated to insure good electrical connection when it is placed in the above equipment. Known lifetime standards are checked daily.

8. Lineage

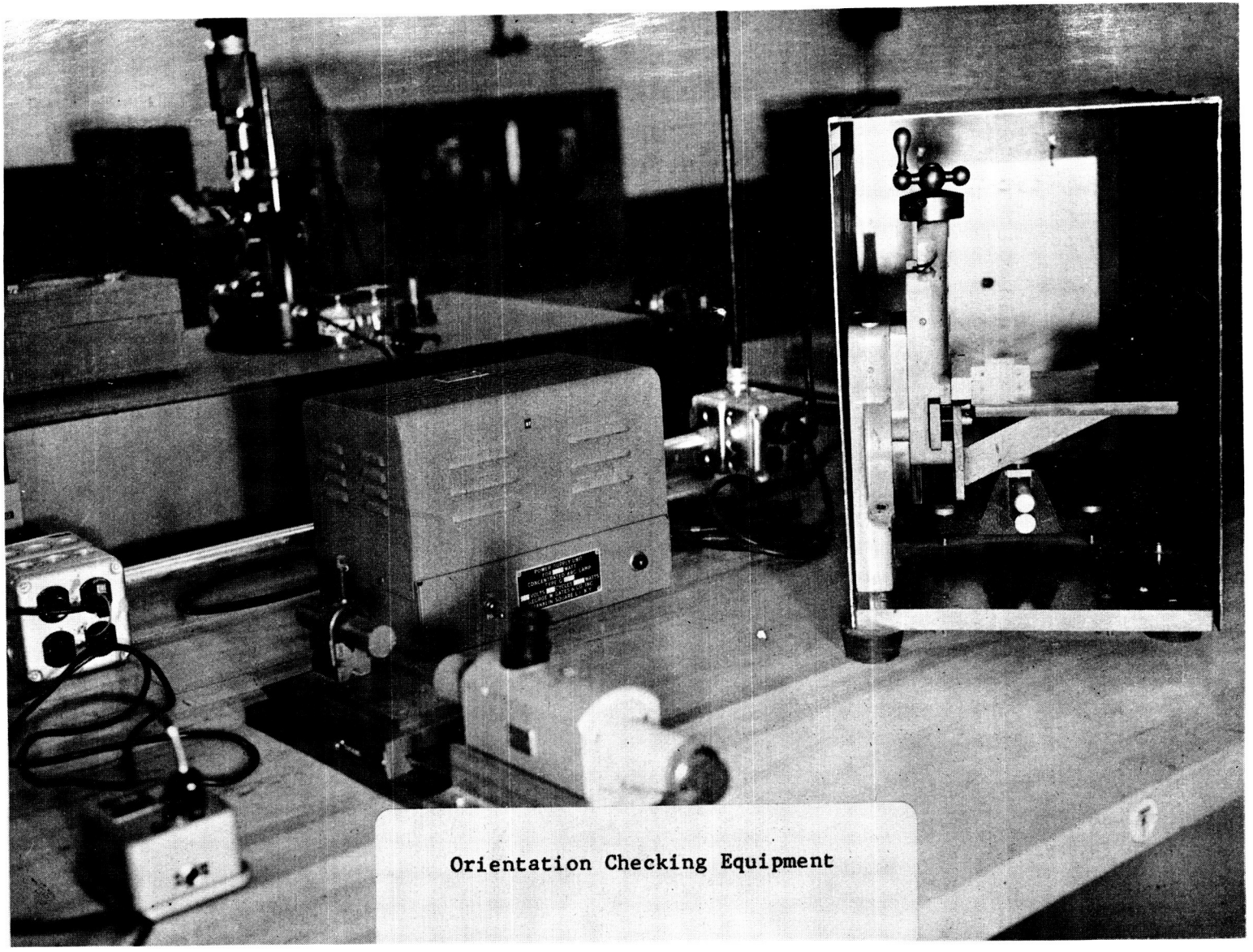
One slice is taken from the end of the crystal opposite the seed. This slice is then lapped using 12 micron grit size. Following lapping it is degreased and cleaned. The slice is then placed in a mixture of HF, H_2O, and Cr_2O_3 (1:1:1) for 5 minutes. The etch pit count is then made at 200X and the count reported in etch pits/cm^2.

9. Other Imperfections

The slice used in (8) is then relapped to remove the etch and is then re-etched but in a 10% solution of sodium hydroxide for a structural elimination of the slice, where the primary imperfection might be -- twin, poly inclusions or slip.

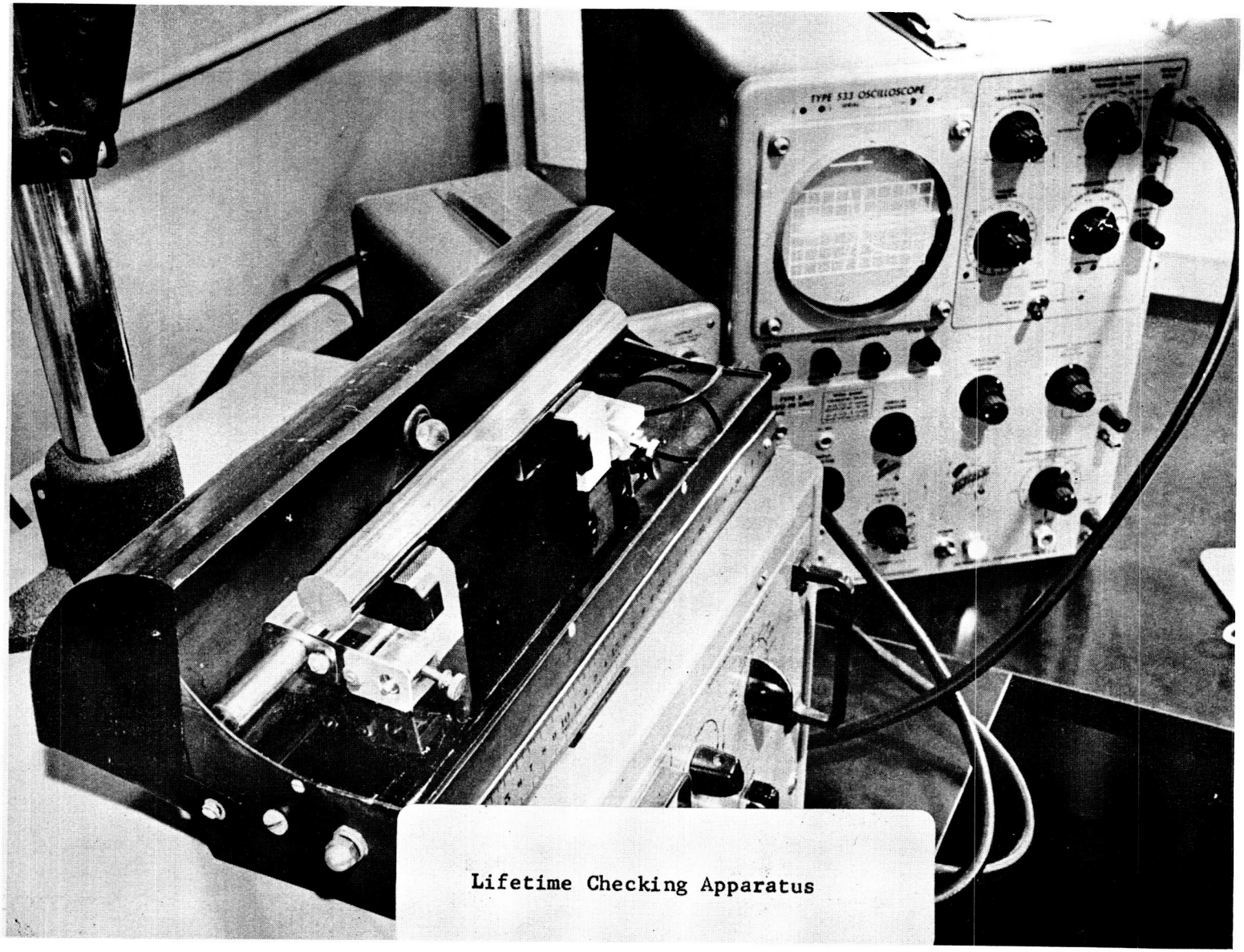
10. After the material has been evaluated and found to be in accordance with specification, it goes to the slicing area. Here the silicon crystal is sliced with a Hamco saw (see Figure 10) which, according to our investigation, gives the best surface finish.

11. The slices are then forwarded to the lapping area where approximately 2 mils are removed from each side of the slice with a Hoffman planatary lapping machine (see Figure 11). The lapping slurry used is approximately 12 micron grit size, which leaves a mat surface.



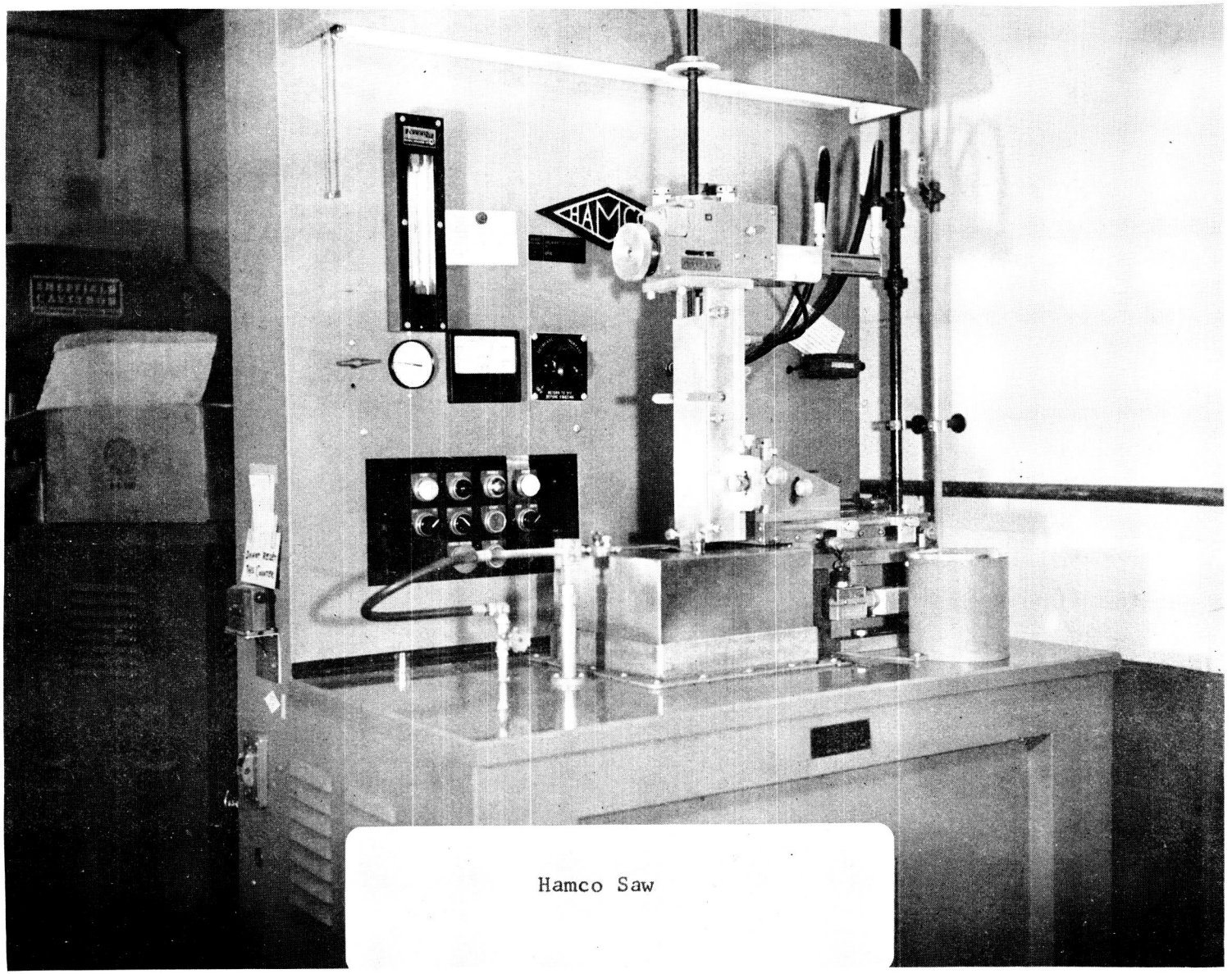
Orientation Checking Equipment

Figure 8



Lifetime Checking Apparatus

Figure 9



Hamco Saw

Figure 10

Hoffman Planatary
Lapping Machine

Figure 11

B. EPITAXIAL GROWTH

1. Background

The present method for producing silicon epitaxial overgrowth on silicon involves a crystallization from the gaseous phase by the aid of the chemical reaction between silicon tetrachloride and hydrogen at elevated temperatures. Similar such processes have been used for the past 100 years for the production of crystals.

The substrate on which oriented crystallization of a single crystal layer takes place need not consist of a crystal identical to the crystallizing substance. This follows from numerous facts concerning epitaxial overgrowth to which many investigations have been devoted since Frankenheim's[1] time. It is sufficient for the lattice of the substrate to possess the necessary metric and energy compatibility with the crystallizing substance or even for its surface to be compatible in metric and energy respects with at least one principal force of the crystallizing substance. The kinetics and regularities of such growth were thoroughly studied by Dankov[2] who formulated the principle of crystallographic correspondence.

The first stage in crystal growth from the vapor phase must be the formation of a nucleus. This is the smallest number of atoms capable of sustaining further growth, units smaller than this tending to evaporate. This requires molecules to condense into clusters and grow until a critical size has been passed. Clearly, if the pressure of the molecules is very high, i.e., if the vapor is supersaturated then there will be increased tendency for the molecules to condense into clusters and grow into nuclei. The supersaturation required for growth of a nucleus may be very high; indeed, it can be shown supersaturations of about 50% may be necessary. Supersaturation is usually defined as α where

$$\alpha = \frac{\rho}{\rho_o} - 1$$

(1) L. M. Frankenheim, Poggend. Ann., 37, 516 (1936).
(2) P. D. Dankov, "Proc. of the Second Conf. on the Corrosion of Metals," 2, 120 (1943).

ρ = pressure of vapor

ρ_o = equilibrium vapor pressure of the condensed phase at that temperature.

Once formed, the nucleus begins to grow. Atoms from the vapor collide with the nucleus, diffuse over the surface until either they find a suitable site or fly off into the vapor again. Atoms condensing on the surface lose latent heat causing the surface to be at a higher temperature than the bulk of the crystal. Surface temperatures 100°C higher than the bulk temperature have been suggested by Wilman[3] as a factor contributing to the mobility of atoms on the surface.

Atoms condensing on the surface will prefer sites with a maximum number of nearest neighbors because at such sites the bonding energy is at a maximum. Occupation of such sites would produce closely packed surfaces over the nucleus. At this point, further condensation becomes difficult. For further growth, sufficient atoms must come together to form an island "nucleus" on the close packed surface. Once formed, the island may grow laterally to the extremities of the surface and then for further growth another nucleus must be formed. This process is similar to the formation of the original nucleus.

The concept of growth by two dimensional nucleation has been considered by several workers and it is possible to estimate the rate of nucleation; i.e., the rate of formation of monolayer islands and also to estimate the degree of supersaturation required to cause detectable growth. The theoretical value of the latter is of the order of 25 to 50%. However, in practice, it has been found that crystals may grow at low supersaturations of about 1%. This anomaly was explained by Frank[4] who proposed the mechanism of crystal growth which follows. He pointed out that if atoms were added onto the steps of a screw dislocation, a close packed surface of the type described in the previous paragraph was never formed but instead a growth spiral resulted. It should be realized that the origin of dislocations and growth spirals is not completely understood. They may be

3. H. Wilman, Proc. Phys. Soc., London, 1368, 474 (1955).
4. F. C. Frank, Disc. Fariday Soc., No. 5, 48 (1949).

created in the nucleus by thermal agitation or mechanical deformation or introduced during subsequent development of the nucleus. This suggests that the dislocation density can be reduced if conditions during growth are made as free from fluctuations (thermal and mechanical) as possible.

Since the substrate acts as an initial "nucleus" in epitaxial overgrowth, it might be expected that the perfection of overgrowth would depend upon the crystallographic orientation of the substrate. This has been observed in germanium where it was found that the rate of germanium overgrowth was dependent on the substrate crystal orientation for the most densely packed faces <110>, <111>, and <100>. Owing to the strong bonding forces acting in the planes of these faces, condensing atoms will be oriented in the correct way.

The perfection of overgrowth also depends on the temperature of the substrate. It has been found that silicon overgrowths prepared at a substrate temperature of 1270°C show a high order of perfection while the overgrowths prepared at 1175°C are less perfect. These results suggest that during deposition, the high surface mobility of silicon atoms attained at 1270°C is essential for good film perfection. The high surface mobility of silicon atoms enables them to diffuse over the surface and to find correct oriented positions.

A further requirement for the preparation of good epitaxial overgrowth is that the substrate must be free from surface defects. For example, in the case of silicon good epitaxial overgrowth cannot be obtained in the presence of a substrate surface oxide. The latter provides nucleation sites for polycrystalline growth.

In the epitaxial overgrowth of silicon, the deposited silicon is produced by the hydrogen reduction of halosilanes such as silicon tetrachloride, the reduction of which may be represented by the simple equation:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl.$$

This equation does not predict the observed yield of other chlorosilane compounds or the yield of high molecular weight polymers of the homologous series $(SiCl_2)_xH_2$, such as $Si_{10}Cl_{20}H_2$, found as a condensate on the reaction walls. To account for the reaction products, it is possible to formulate numerous equations which represent possible reaction mechanisms. The standard free energies for a few of these reactions have been calculated (see Table I) and it may be seen that all are thermodynamically possible. An investigation has been carried out to evaluate, by means of gas chromatography, the reaction products of the silicon tetrachloride and hydrogen reaction.

It has been found that the epitaxial overgrowth rate of silicon is effected by the hydrogen to silicon tetrachloride molar ratio and also the hydrogen flow rate. The causes for these effects are not understood completely. It has been suggested that owing to the relatively high activation energy found for the hydrogen-silicon tetrachloride reaction and reduction in growth rate found by increasing the molar ratio above 0.1 that the following mechanism is possible. First there is adsorption of a silicon subchloride, probably the free radical $SiCl_3$, on the substrate surface and this is followed by loss of chlorine by reaction with hydrogen. However, the occurrence of adsorption phenomena at high temperatures seems doubtful and until further work has been carried out, particularly on the identification of reaction products, the kinetics of the reaction of hydrogen with silicon tetrachloride will remain obscure.

2. Requirements for Epitaxial Growth

The power integrated circuit design consisted of an N^+ layer deposition of 10^{19} atoms/cc followed by a deposition of an N^- layer of 10^{15} atoms/cc. This two-layer structure requires careful material preparation techniques and epitaxial procedures to minimize surface defects. It has been determined that all epitaxial defects originate at the substrate epitaxial layer interface and are dependent on surface cleanliness, surface perfection and epitaxial system purity.

TABLE I

Standard Free Energies for
Typical Silicon Reactions

Reaction	Standard Free Energy for reaction at 1553Å (1270°C)
$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl$	-1.9 Kcal/mol.
$SiCl_4 + Si \rightleftharpoons 2SiCl_2$	-2.2
$SiCl_2 + H_2 \rightleftharpoons Si + 2HCl$	-1.2

a. Substrates: The substrates used for the power integrated circuit design were P-type 20 ohm-cm. The doping level of the substrate was selected.

Doped substrates inherently can contain sufficient impurities to distort the crystal lattice. Distortions caused by precipitates or inclusions will not permit a sufficiently good lattice match for defect-free epitaxial growth. These distortions can be eliminated by careful selection of the parent crystal growth conditions and the type of dopant. Evaluation of the substrate material is accomplished by examination of the chemically polished surface prior to epitaxial growth. A chemically polished surface was employed for this device to insure a damage-free surface and to permit microscopic examination of the surface before growth was initiated.

b. Substrate Preparation: Preparation of the substrate material before epitaxial growth is a deciding factor in producing defect-free epitaxial layers. Heavy metal impurities, such as aluminum or iron, are retained by the substrate after the slicing and doping operations. These can give rise to foreign nucleation sites during the growth process. Wetting agents or solvents do not effectively remove these heavy metals. However, chemical techniques, such as reactive chloride acids, convert most heavy metals to water soluble metal chlorides and are easily removed by subsequent rinsing in deionized water.

c. Epitaxial System Purity: Epitaxial growth perfection is also dependent on system purity, that is, the environment in which the chemical reduction of the halide takes place.

Gas system -- The gases used in the epitaxial process must be of good quality. The hydrogen used for the reduction is passed through a Deoxo unit to remove traces of oxygen and then through a dryer to remove water to a purity of less than 1ppm. All gases are filtered through submicron filters to remove foreign particles before they enter the reaction chamber.

The control of the gases, the valving and piping required to mix and dilute, switching and metering are all done in a system that is leak proof. The materials of construction are Teflon and quartz to maintain gas purity prior to the reaction chamber.

Reactor -- A horizontal RF heated epitaxial system was used for all the power integrated circuit substrates (Figure 12). The susceptor was a pure grade of graphite coated with silicon carbide. The silicon carbide is deposited on the graphite under the same conditions required for epitaxial growth to insure a noncontaminating or defect contributing source.

The reactor tube was of quartz and the susceptor is supported on a quartz sled. Reactor tube and susceptor loading is accomplished in a positive pressure hood to minimize dust or environmental particles from contaminating the surfaces of the slices.

Epitaxial procedure -- The epitaxial procedure for the power integrated circuit device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse of the deposition reaction and permits the removal of the last traces of work damage caused by chemical polishing.

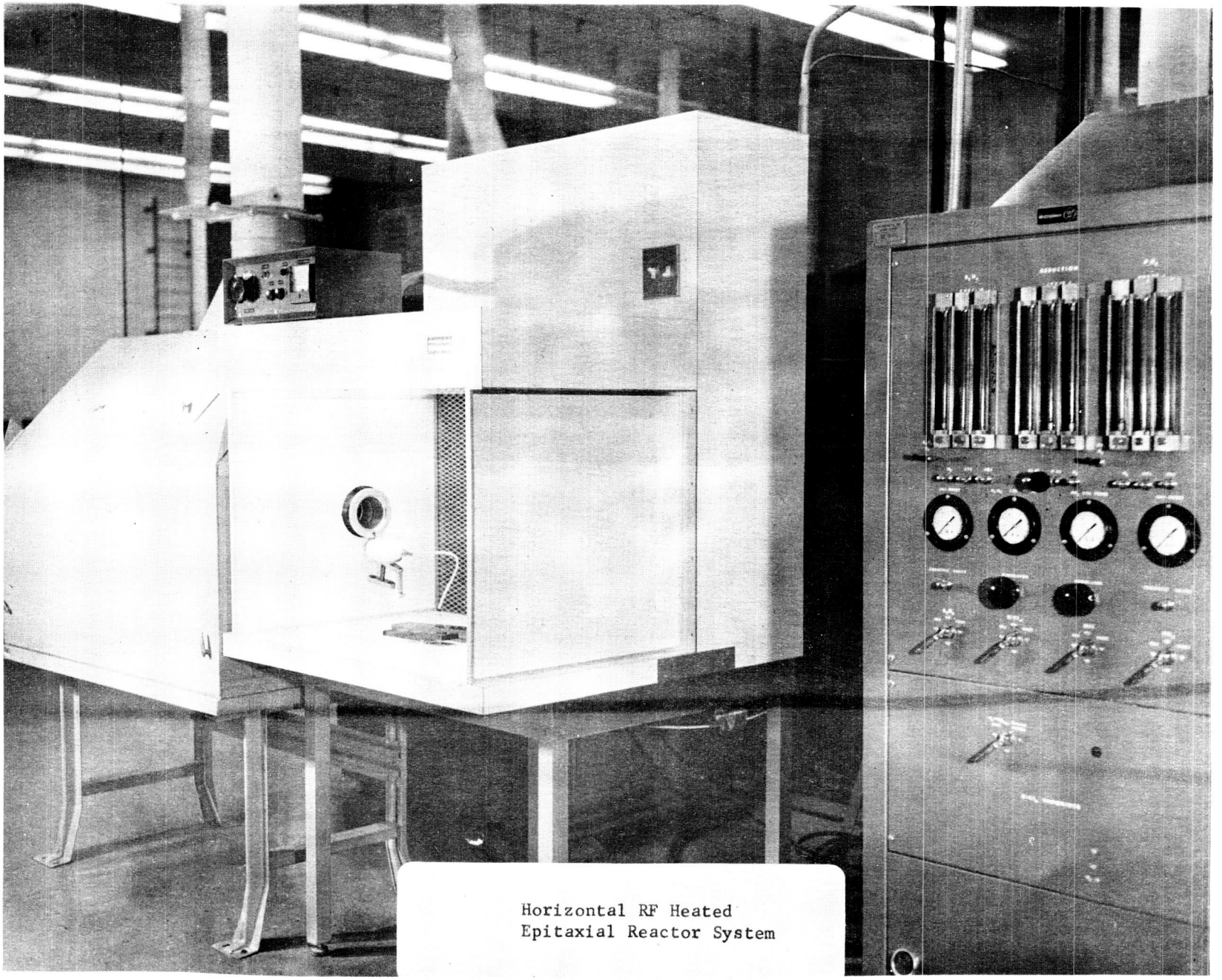
$$4HCl + Si \longrightarrow SCl_4 + 2H_2$$

Sufficient silicon is removed to insure a lattice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. The N^+ deposition follows for the designed thickness and the concentration is controlled to 10^{19} atoms/cc. After the N^+ layer has been deposited, the system is purged with pure hydrogen at 1200°C to remove the residual traces of the reactant gases from the reactor. The N^- layer deposition then follows to give a layer of 25μ of N, 5 ohm-cm. Gaseous dopants such as phosphine and arsine are used to control the resistivity in the epitaxial layers. After the growth of the N^- layer the system is cooled for removal of the substrates.

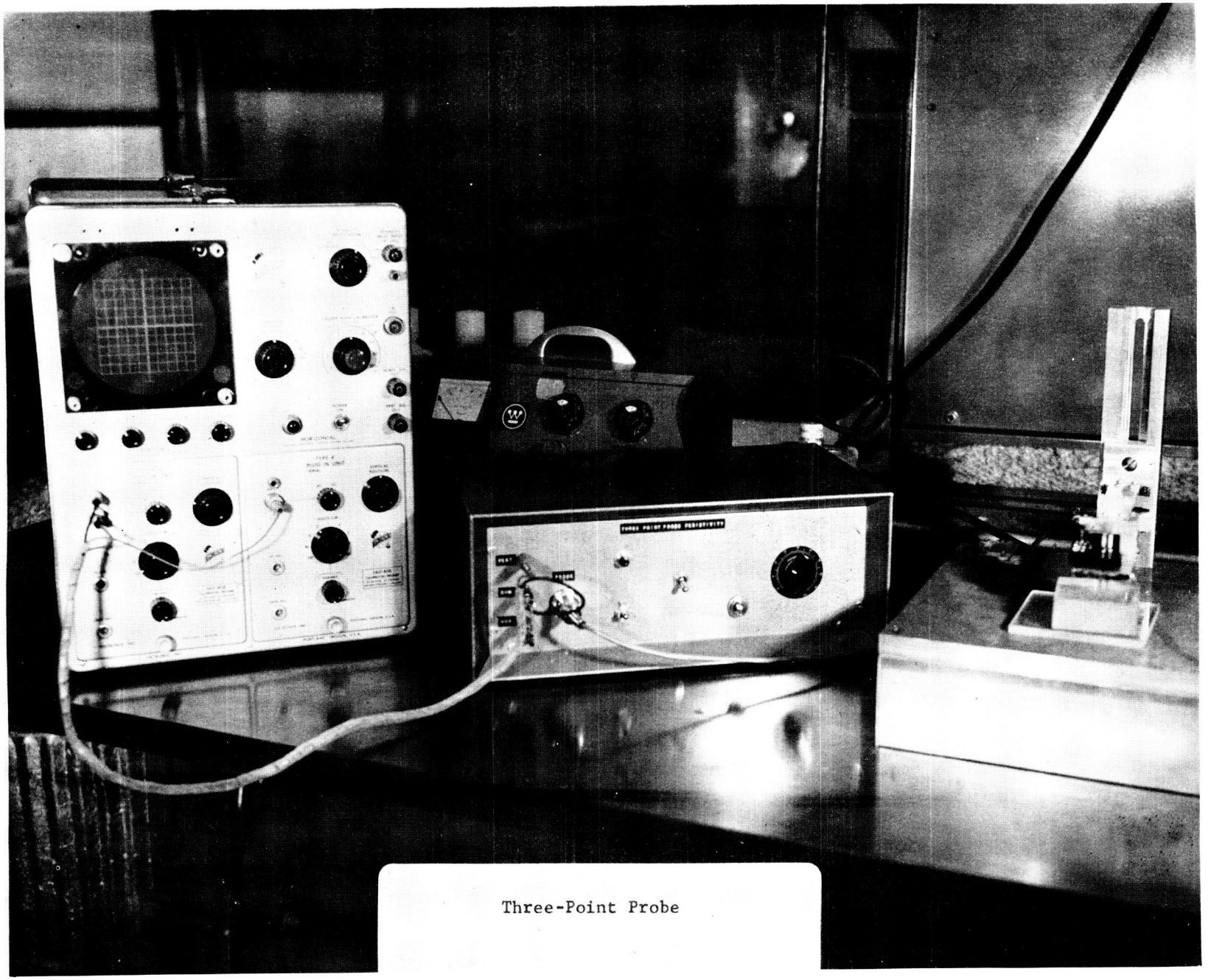
3. Evaluation of Epitaxial Layer and Substrate Material

a. Resistivity: The resistivity of the grown layers was determined using a three-point probe and a four-point probe (Figures 13 and 14).



Horizontal RF Heated
Epitaxial Reactor System

Figure 12



Three-Point Probe

Figure 13

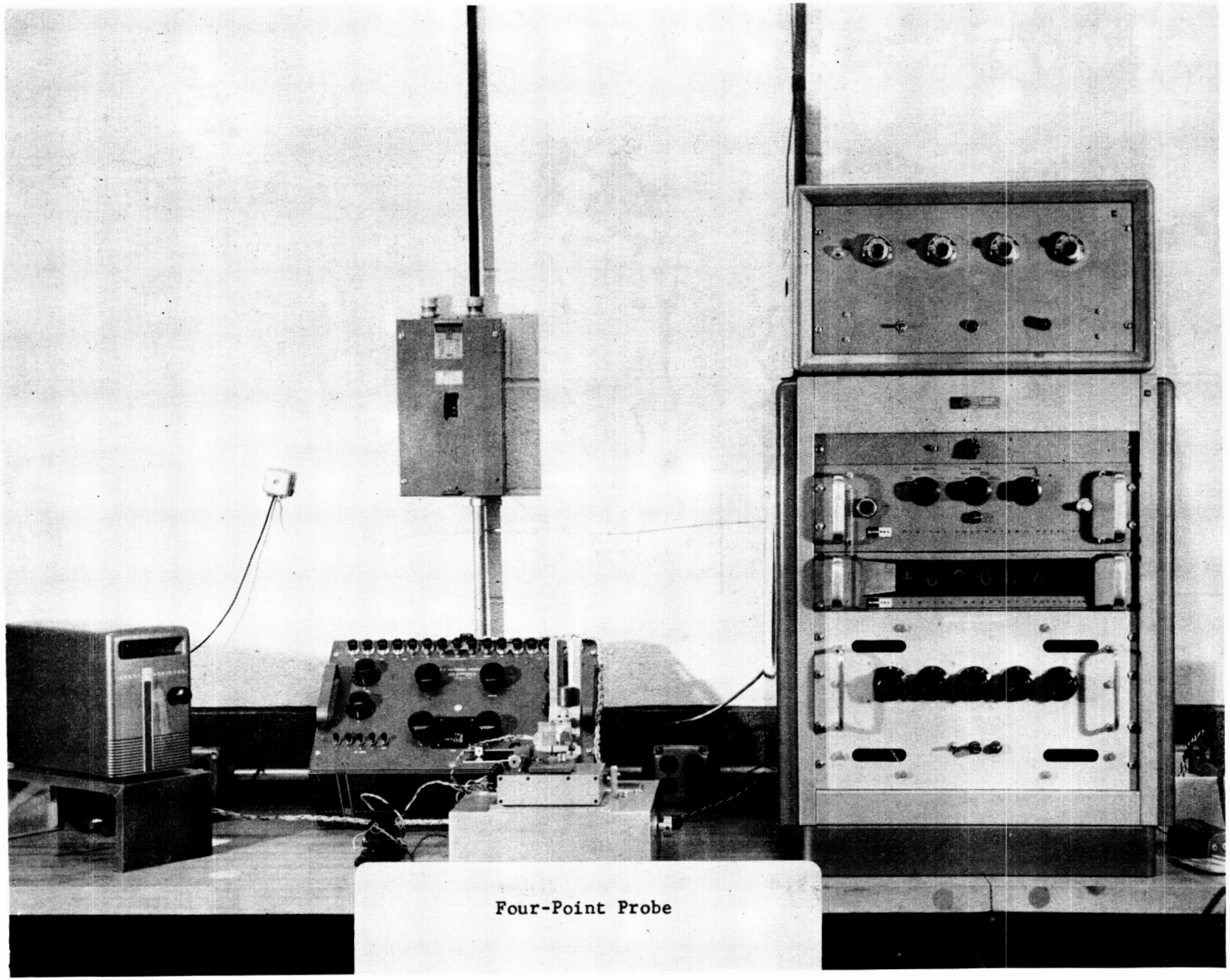


Figure 14

The N^- layer resistivity was determined by three-point readings on a single N^+N^- deposition.

b. Layer Thickness: The thickness of the deposited layers was accomplished by angle lapping and staining techniques. Interference measurements with sodium light were used to determine actual layer thicknesses (Figure 15).

c. Surface Quality: Visual examination, microscopic techniques, and chemical etching of the surface were used for surface evaluation. If any defect was found under visual examination of the active area of the deposited substrate, the slice was rejected (Figure 16). Units fabricated from slices containing poly inclusions on tetrahedrals always gave low voltages.

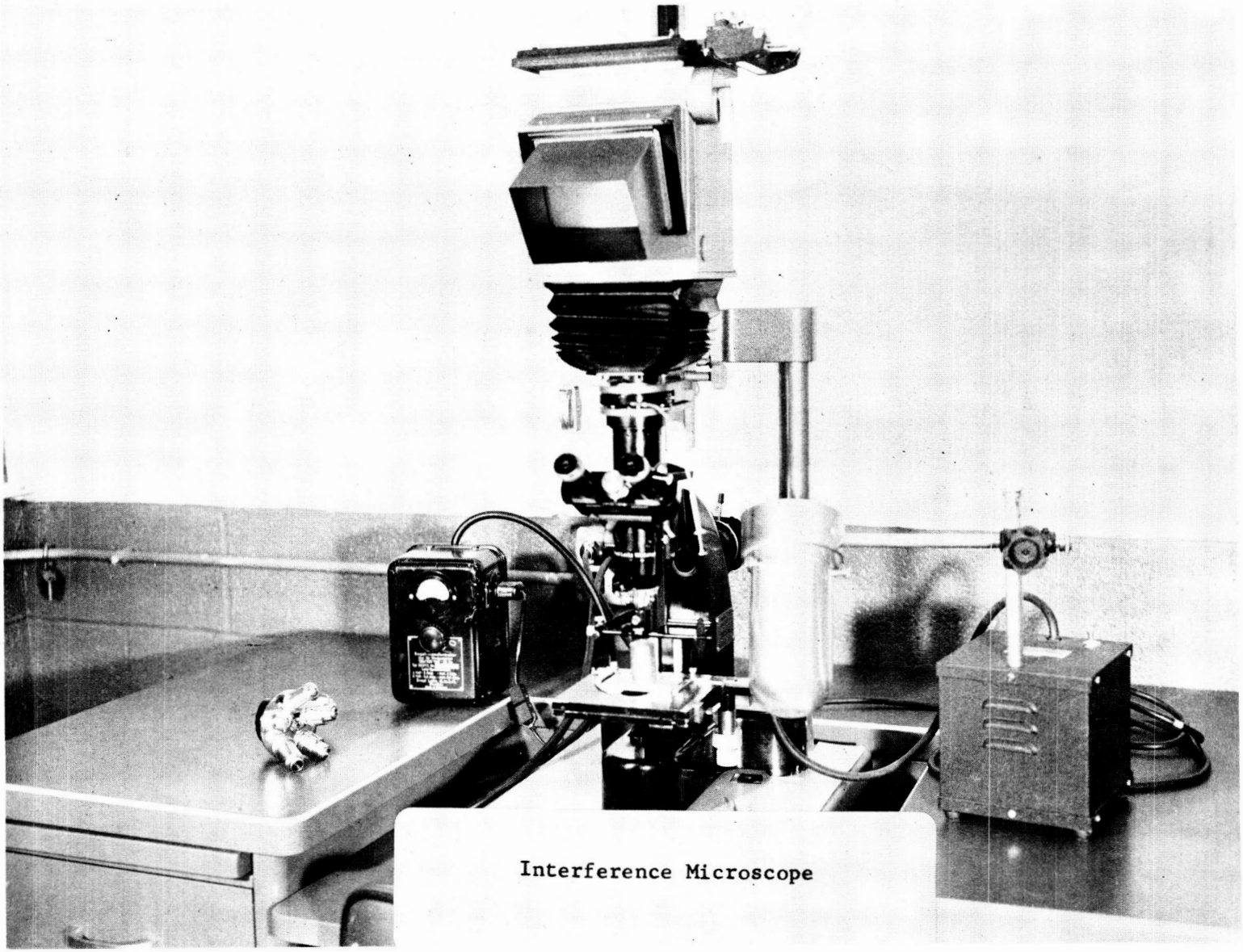
The surfaces were also etched in a chromic oxide, hydrofluoric acid, water mixture to determine the number of stacking faults present. Counts of 8-20 per cm^2 were the usual case.

C. DIFFUSION

O_2 and N_2 are the two process gases used for diffusion. The high purity house gases are further purified by being passed through a molecular sieve and a 0.4μ Millipore membrane filter. The gases are piped to the diffusion furnace in stainless steel tubing. Immediately prior to entering the diffusion furnace the gases are passed through a cold trap at dry ice temperature. All diffusions are done from inside a Westinghouse designed clean room with controlled humidity, temperature and dust count. Prior to each diffusion the wafers are given a thorough pre-diffusion cleaning, as outlined below:

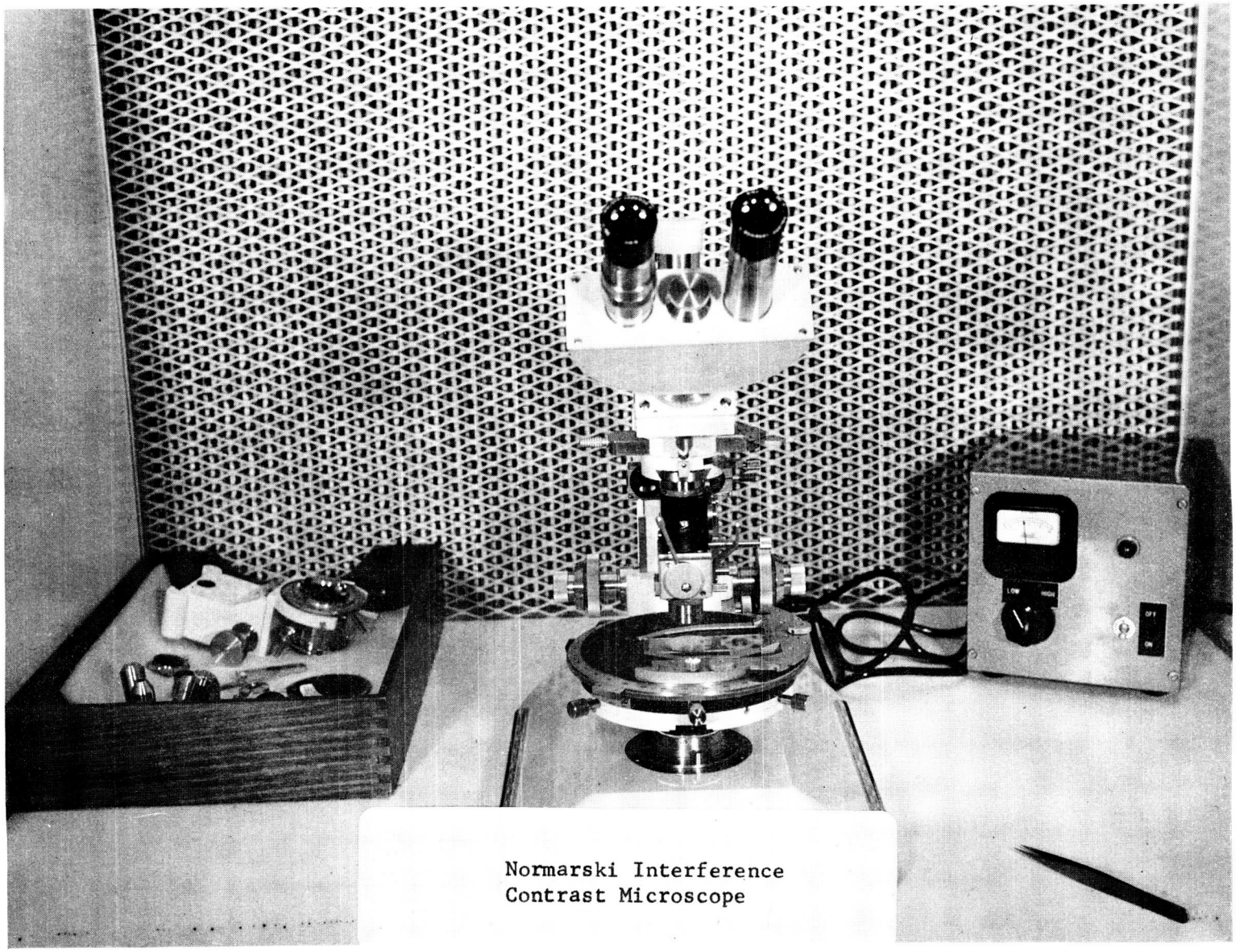
Pre-diffusion Clean

1. Hot sulfuric acid -- 15 minutes
   Temperature -- 250°C
2. Rinse deionized water -- 5 minutes
3. Hot nitric acid -- 15 minutes
   Temperature -- 200°C
4. Rinse deionized water -- 10 minutes



Interference Microscope

Figure 15



Normarski Interference
Contrast Microscope

Figure 16

5. Hot triple-distilled water -- 5 minutes
   Temperature -- 80°C
6. Second hot triple-distilled water -- 5 minutes
   Temperature -- 80°C
7. Blow dry from hot water immediately prior to diffusion.

Figure 17 is a photo of the clean room diffusion area.

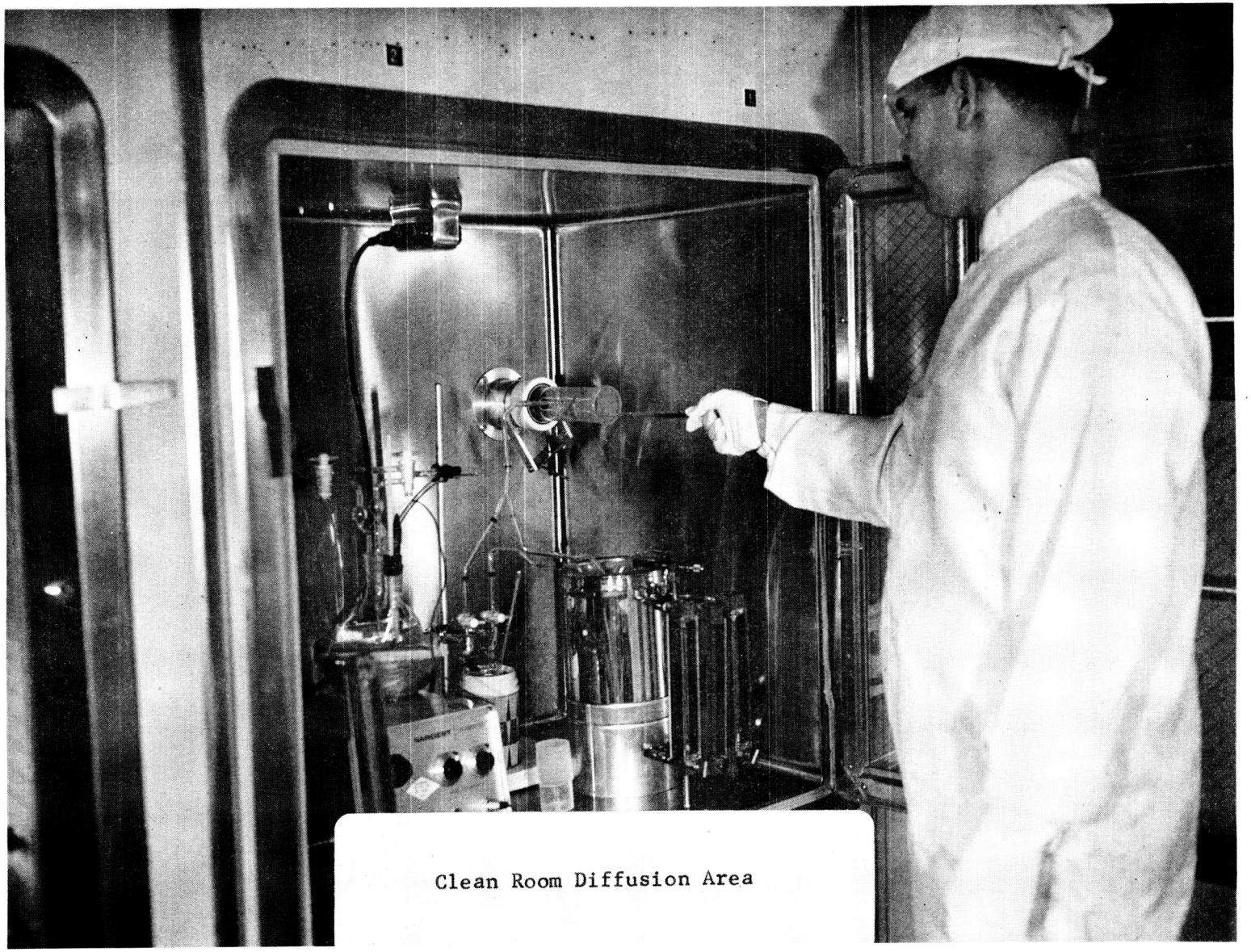
The initial oxidation is done at 1200 ± 1°C for two hours in a steam atmosphere. This produces a 10,000 ± 500Å layer of SiO_2. Initially only 7,000Å of SiO_2 was grown. The oxide thickness was increased because premature breakdown of the collector emitter junction was observed.

The base and resistor diffusion is a two step, deposition and drive, operation. A 20 minute, 1000 ± 1°C $BBr_3(g)$ deposition, in an atmosphere of O_2 and N_2. This yields a sheet resistivity of 40 ± 5 Ω/□ . This deposition is followed by a 90 minute, 1200°C drive in a steam atmosphere producing an X_j of 4.5 ± 0.6μ and a sheet resistivity of 125 ± 20 Ω/□ . The SiO_2 grown during this operation serves as a diffusion mask for the emitter and collector diffusion.

The emitter diffusion is done at 1150 ± 1°C in an atmosphere of $POCl_3(g)$, O_2 and N_2 for a time dependent on the initial base junction depth. The resulting sheet resistivity is 2.0 ± 0.5 Ω/□ , the emitter X_j is typically 3.3 ± 0.3μ, the W_B 3.2 ± 0.4μ. This diffusion operation also provides the N^+ collector contact area. Following the emitter diffusion, the wafers are oxidized in a steam atmosphere for 10 minutes. At this temperature the junction depths do not change. The purpose of this operation is to provide surface stabilization and to dilute the P_2O_5 "glass" formed during the emitter diffusion. This prevents undercutting during contact etching, since this undercutting might be caused by the difference in etch rates between the P_2O_5 "glass" and SiO_2.

D. PHOTORESIST

All photoresist is done inside the clean room. The photoresist operations are as follows:



Clean Room Diffusion Area

Figure 17

Coating

1. Coat with 2:1 KMER
2. Spin for 45 seconds, 3000rpm
3. Bake 10 minutes in 95° oven

Photomask

1. Align appropriate mask
2. Expose for 20 seconds
3. Spray with developer for 30 seconds
4. Spray with propanol alcohol for 30 seconds
5. Spray with nitrogen air for 30 seconds
6. Bake 30 minutes in 150° oven

Etch Oxide

1. 6:1 oxide etch
    a. 6 -- ammonium fluoride
    b. 1 -- HF
2. Etch for 5-6 minutes until oxide is removed, rinse deionized water, air dry nitrogen
3. Remove photoresist
    a. Hot sulfuric acid - for 20 minutes; temperature 500
    b. Place second sulfuric acid - for 15-20 minutes
    c. Rinse deionized water - 5 minutes
    d. Place hot deionized water - 20 minutes; temperature 80°C
    e. Place second deionized water - 20 minutes; temperature 80°C
    f. Air dry nitrogen

Aluminum Etch

1. Aluminum etch -- 400 phosphoric, 40 nitric, 100 H_2O
2. Etch until aluminum is removed from inverse contact areas
3. Rinse in deionized water
4. Air dry nitrogen

Silicon Etch

1. Si etch - 15 HNO_3:5HAc:3HF
2. Etch until isolation groove reaches substrate
3. Rinse in deionized water
4. Air dry in N_2

It is difficult to etch a groove two mils deep into a polished Si surface with the tolerances required.

The problem is one of depositing a photoresist film which will adequately resist both an oxide etch and a silicon etch. This problem has been solved by using concentrated KMER. The resist is applied to the wafer by

conventional spinning techniques (3500rpm for 30 sec). After curing the resist at 95°C for 10 minutes, the correct groove etch mask is aligned to the wafer and the resist is exposed with ultraviolet light. Following standard KMER developing procedures, the image is thoroughly inspected and baked at 150°C for 30 minutes. This bake cycle has been found to give the best protection in the oxide etch. The wafer is then submersed in the NH_4F-HF etch until all the oxide is removed from atop those areas where the isolation groove is to be etched. Next the resist is stripped from the wafer and a new coating is applied as outlined above. However, to provide the maximum acid resistance to the Si etch, the resist is now baked at 120°C for 20 minutes. The exposed Si is etched in a nitric, acetic, and hydrofluoric acid mixture until isolation is completed. During this etching, the back side of the wafer is protected with wax to prevent it from being etched. To check for completion of the isolation, the following test is performed: 1) a physical section is made to insure the etched groove penetrates the substrate; 2) isolation voltage is measured, collector to collector; typically this is greater than 200 volts.

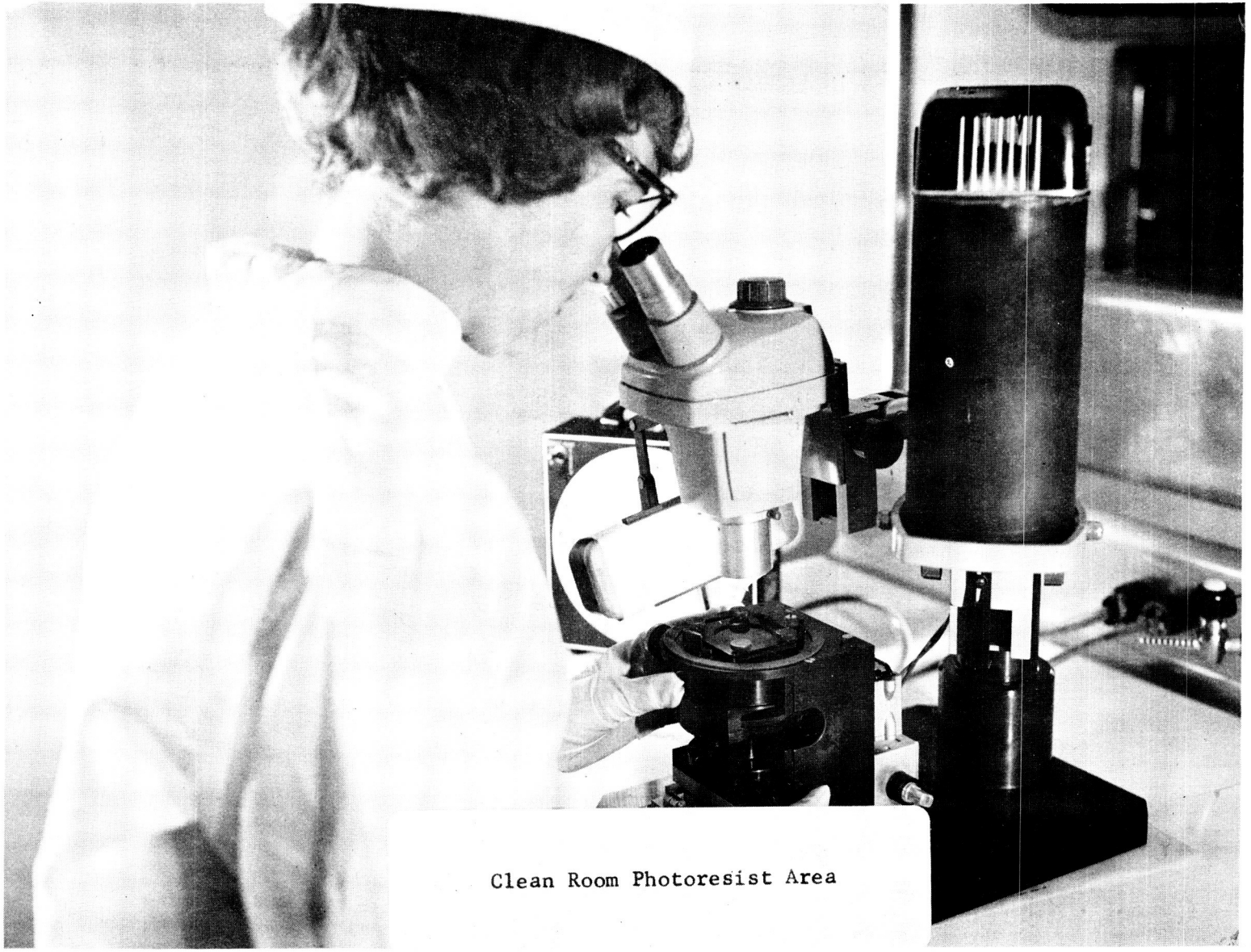
Figure 18 is a photograph of the clean room photoresist area. Figure 19 is a photograph of a 20-watt oscillator wafer after inverse contact masking and etching.

E. METALLIZATION

After contact masking and etching 40,000Å of Al is evaporated onto the wafers. Figure 20 is a photo of the evaporator. The wafers are placed in a vacuum chamber. The vacuum is maintained at less than 10^{-6}mm of Hg during evaporation. An internal resistance heater is used to raise the wafer temperature to 500°C. This insures the clean surfaces necessary for adhesion. The wafers are allowed to cool to less than 100°C before evaporation. After inverse contact masking and Al etching the Al is alloyed at 610 $\pm$ 5°C for 2 minutes.

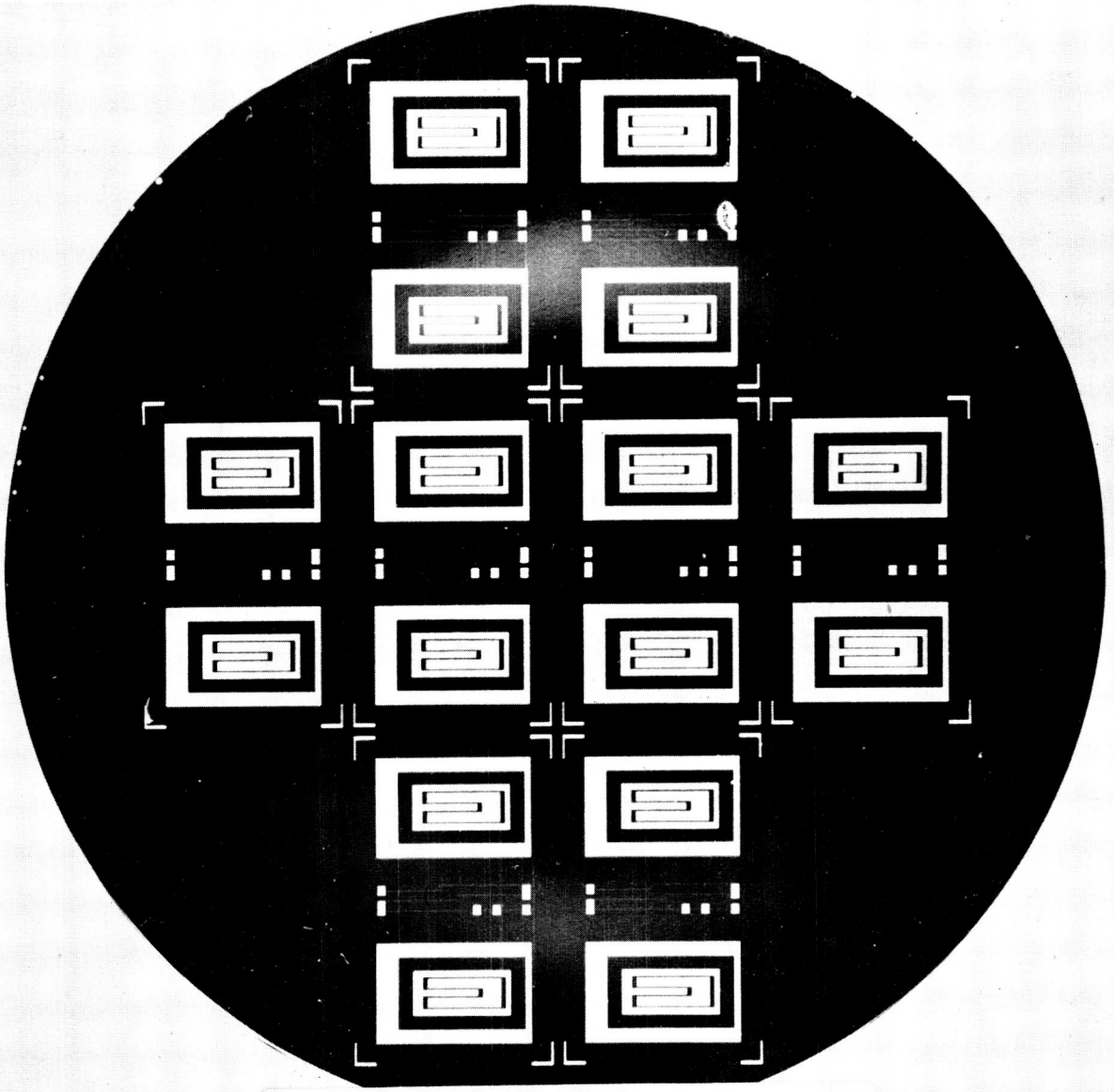
F. ENCAPSULATION

Initial encapsulation studies were made with the 70-watt oscillator in a large, stud mounted package. The final samples of the 20-watt oscillator



Clean Room Photoresist Area

Figure 18



20-Watt Oscillator Wafer After
Inverse Contact Masking and
Etching

Figure 19

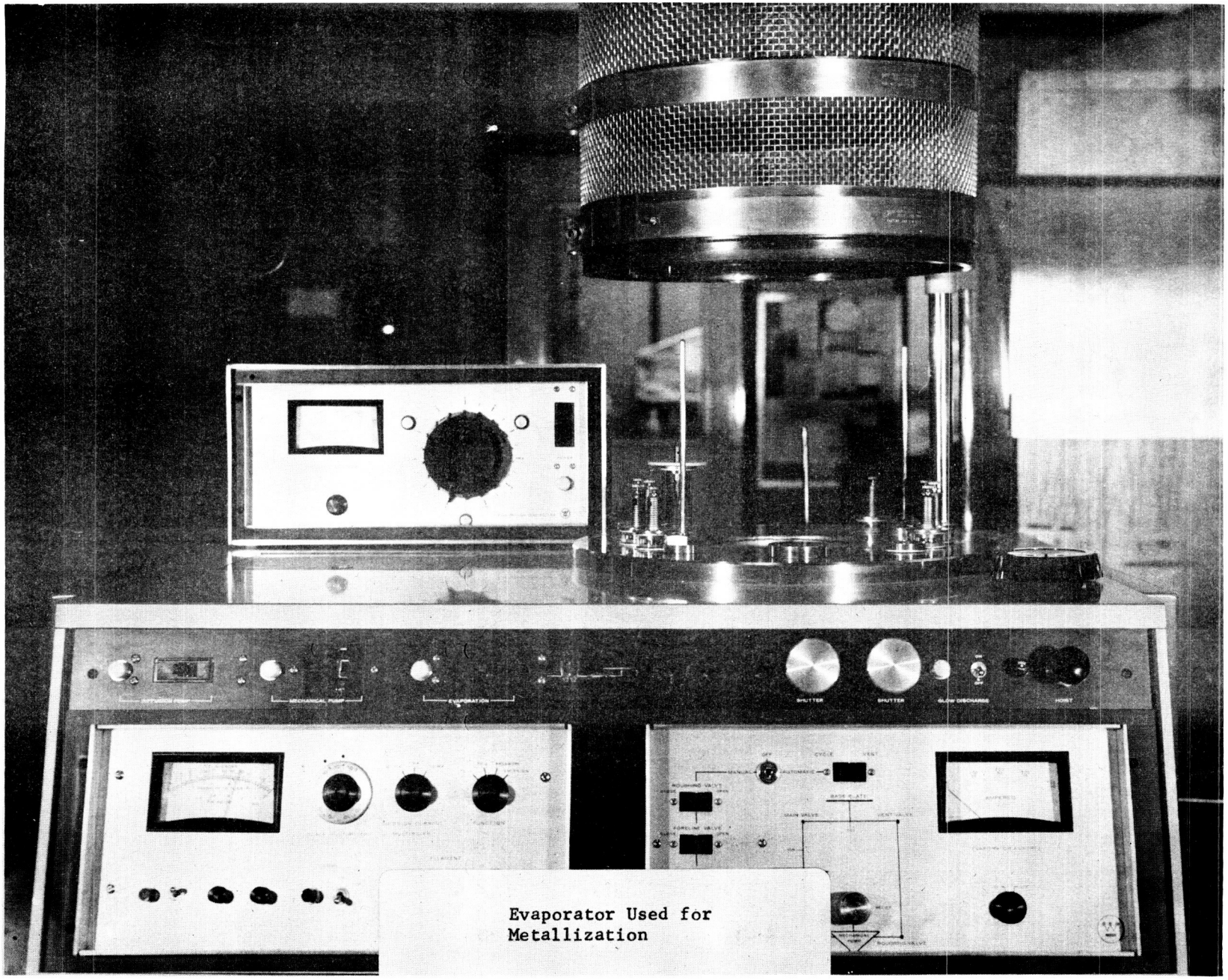
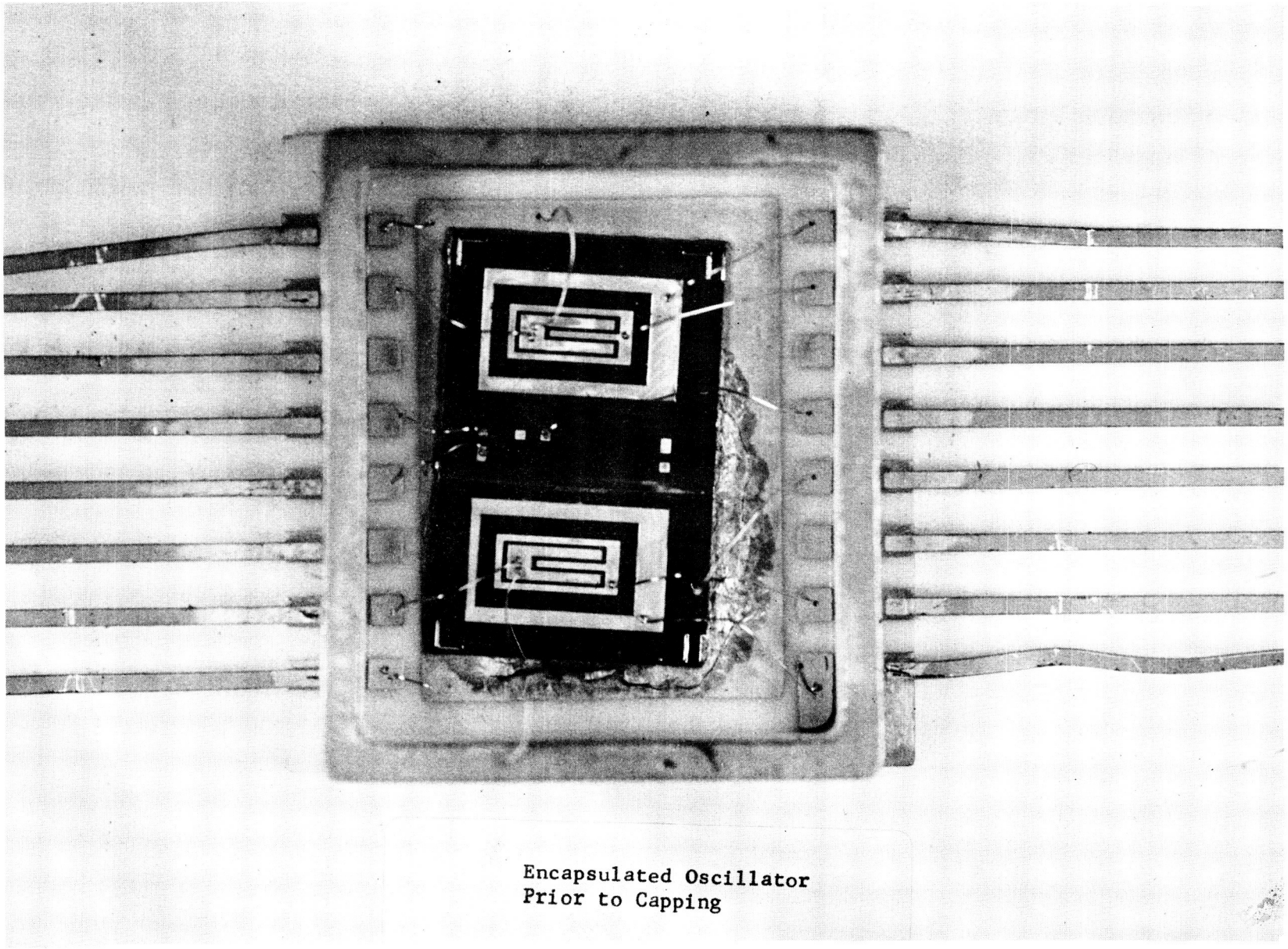


Figure 20

were encapsulated in a new Coor's beryllia flat pack (Coor's package No. A-1212-88-CS) containing 16 leads. This package has a gold metallized ceramic base for mounting of the unit using a Au-Ge preform. Au leads of 2.5 mil are attached using thermal compression bonding techniques. Figure 21 shows an encapsulated oscillator just before the lid is to be put on. The lead arrangement shown is the most logical for the internal connections, but not necessarily for external circuit connections.

There is a redundancy in the emitter connections, since the emitters are tied together and only one lead would be necessary. The diodes in series with the collectors are those formed at the P-type substrate and N-type epitaxial junction. In the mesa approach used for the 20-watt final samples, these diodes are contacted by a lead from the emitter to the Au metallization on the package. This area makes ohmic contact to the substrate via the Au-Ge preform used for wafer bonding. To insure the success of this approach, the backs of the wafers are not protected during the isolation groove etch. This insures that any diffusion that may have penetrated the oxide is etched away. It also insures a polished surface for wafer mounting. Contrary to expectations, it was found that bonding is more successful on a polished rather than on a sandblasted surface.

This technique of bonding a wire to the metallized Au area illustrates the advantage of a ceramic package, i.e., the unit remains electrically isolated from the package. The encapsulated unit meets the environmental objectives. However, the package is so new that detailed thermal dissipation data is not yet available. The device had a thermal dissipation of 10°C/watt (on a heat sink). This is typical of integrated circuit flat packs and causes no difficulties for 20-watt operation.



Encapsulated Oscillator
Prior to Capping

Figure 21

IV. TESTING AND CIRCUIT ANALYSIS

The testing of the Power Integrated Circuit (PIC) units and the circuit analysis was done by the Application Engineering group.

Saturable core transformer type oscillators typically have good efficiencies. This type of network was therefore a good choice for the basic circuit. Efficiencies of approximately 90% were expected. Major losses were primarily of three types -- 1) transistor saturation losses, 2) biasing losses and 3) switching losses.

A. EQUIPMENT

Equipment for taking efficiency data was set up. It consisted of the following:

1. Ballantine True RMS Voltmeter Model 320A

This instrument is considered to be the most critical of the setup. It provides an accurate RMS output voltage reading. A true RMS value of the square wave output is difficult to obtain with any other type of meter. This is important in obtaining an accurate output power value. This is especially true since the equation $P = \frac{V^2}{R}$ was used to calculate output power so that any error in V would be squared, resulting in large errors in the power value. The output resistor was accurately measured on an impedance bridge. It is felt that the RMS meter gives output power values which are much more accurate than any obtained from oscilloscope measurements.

2. Hewlett Packard DC Null Voltmeter Model 413A

This meter was used to accurately measure the DC input voltage to the oscillator circuit.

3. Triplett 0-1A DC Ammeter

This meter was used to measure input current to the oscillator.

4. Tektronix Dual Trace Oscilloscope

This was used to determine when porper operation and correct oscillation frequency was obtained as well as being used to analyze circuit operation.

The diagram of the efficiency testing setup and photographs of the equipment are shown in Figures 22, 23, and 24.

B. RESULTS OF INITIAL TESTING

Efficiency tests were run on several of the first PIC units constructed. These units had beta values of about ten. The PIC units were inserted into the original circuit. Oscillation was obtained at supply voltages of 27 to 28 volts DC. The efficiencies obtained were in the 75 to 85% range.

Efficiency could be increased appreciably by adding several ohms of resistance in series with the feedback coils (see Figure 25 and test data). During the testing procedure, with these resistors inserted, it was noted that current was flowing in both directions through the resistor. This, in addition to the low efficiencies obtained from the original circuit gave evidence that the circuit was not operating properly. An analysis of the circuit operation was initiated.

C. CIRCUIT ANALYSIS

It was determined that reverse breakdown of the emitter base junction of the off transistor was occurring. It can be seen from Figure 26 that this would allow large amounts of base current to flow, thus allowing the circuit to oscillate with low β transistors, where oscillation would probably not occur otherwise.

The low efficiencies were obtained because of the large base currents. Since the emitter base junction held its breakdown voltage, with the large base currents, a considerable amount of energy was being dissipated in this junction.

If the original circuit configuration is used, the number of feedback turns must be reduced until the voltage generated on each feedback coil is less than one half of the emitter-base breakdown voltage. This "one half"

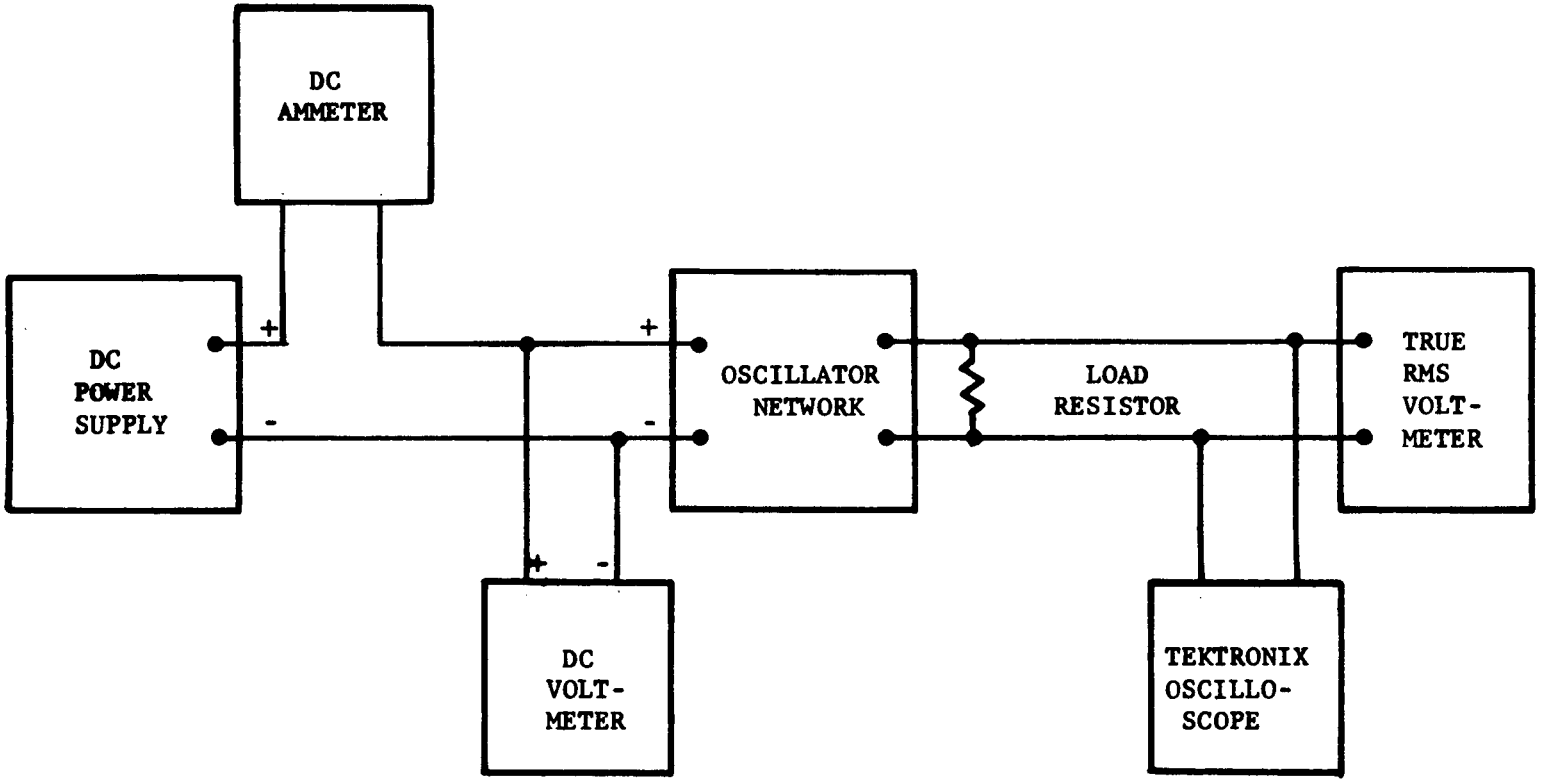
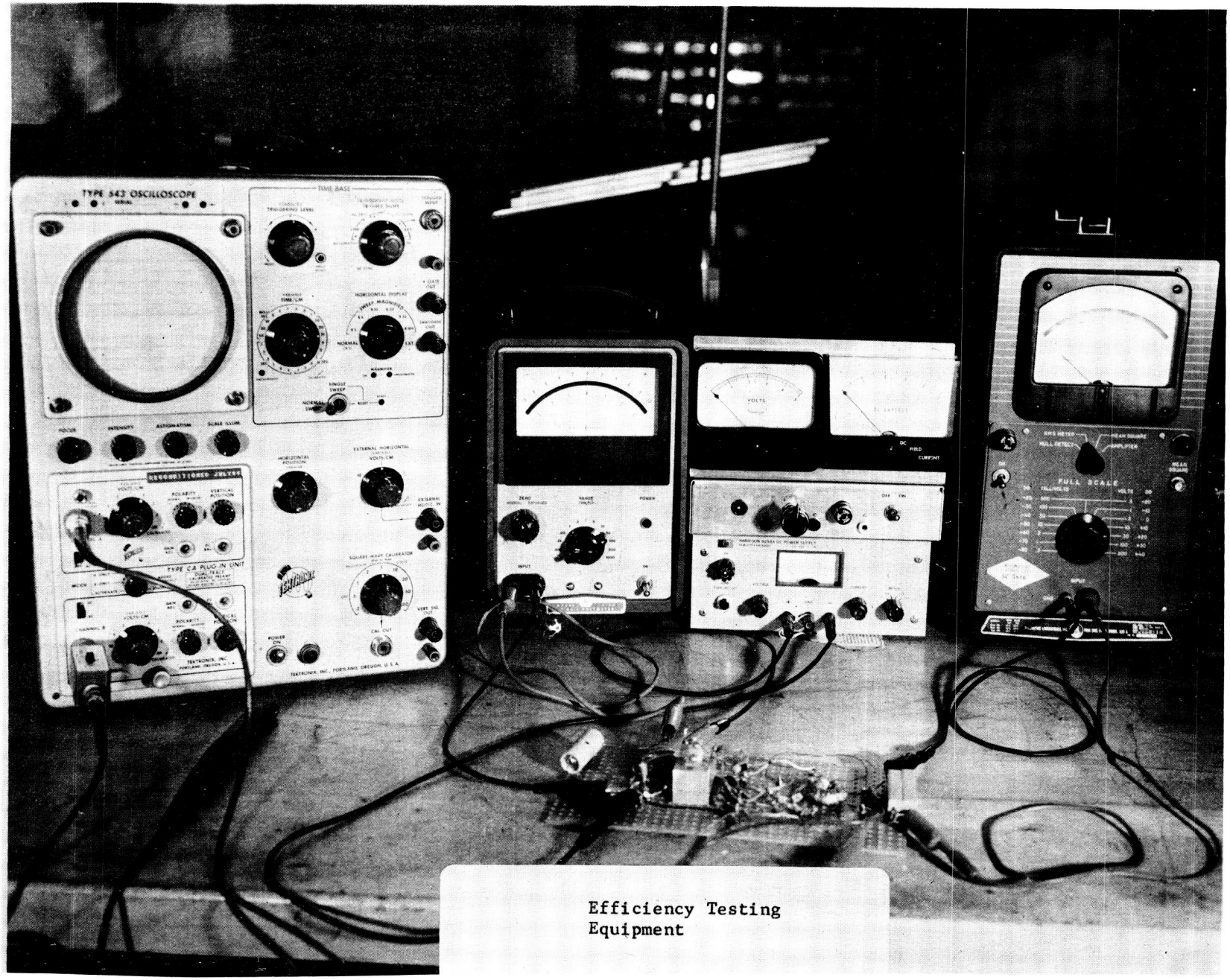
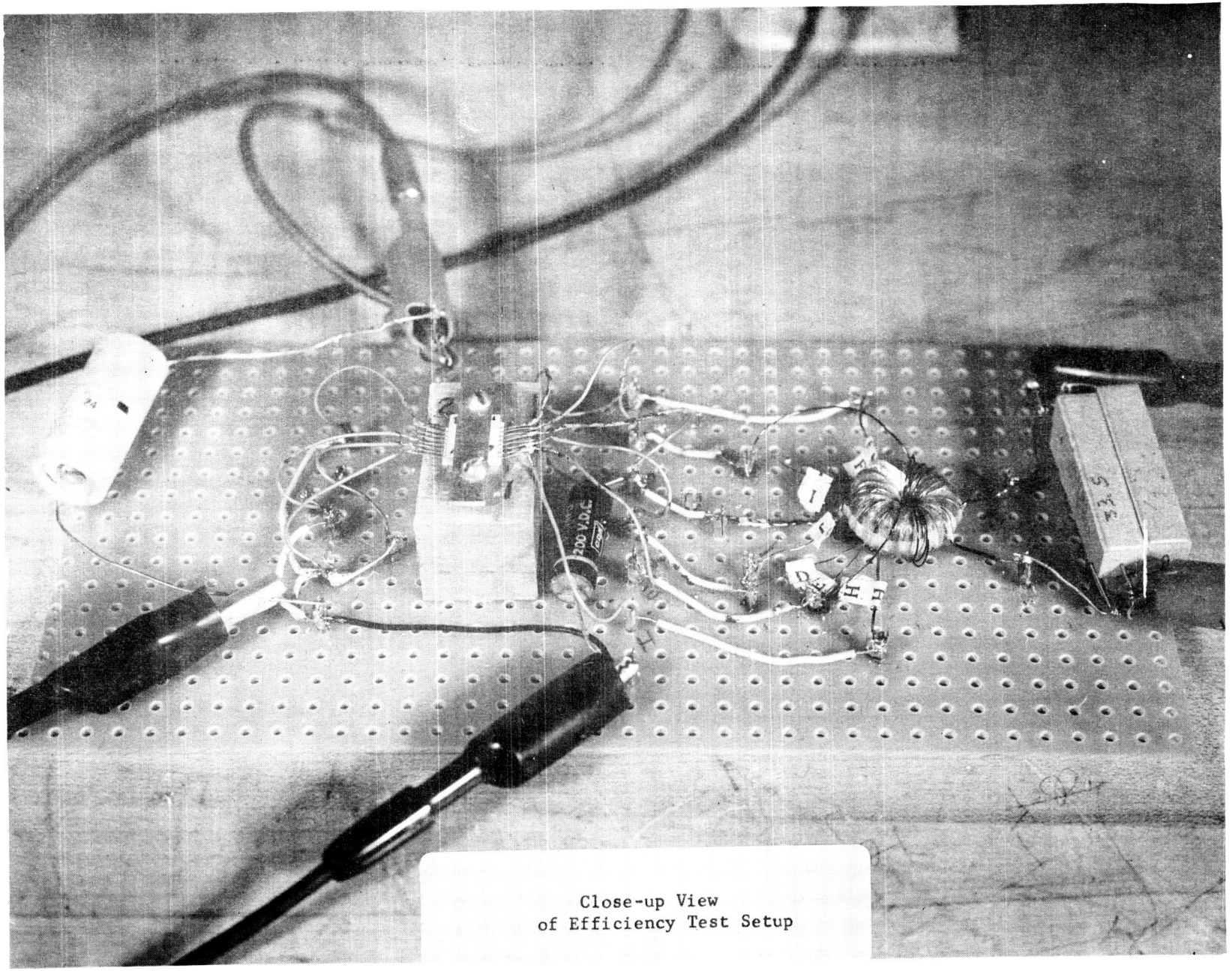


Figure 22: Diagram of Efficiency Test Setup



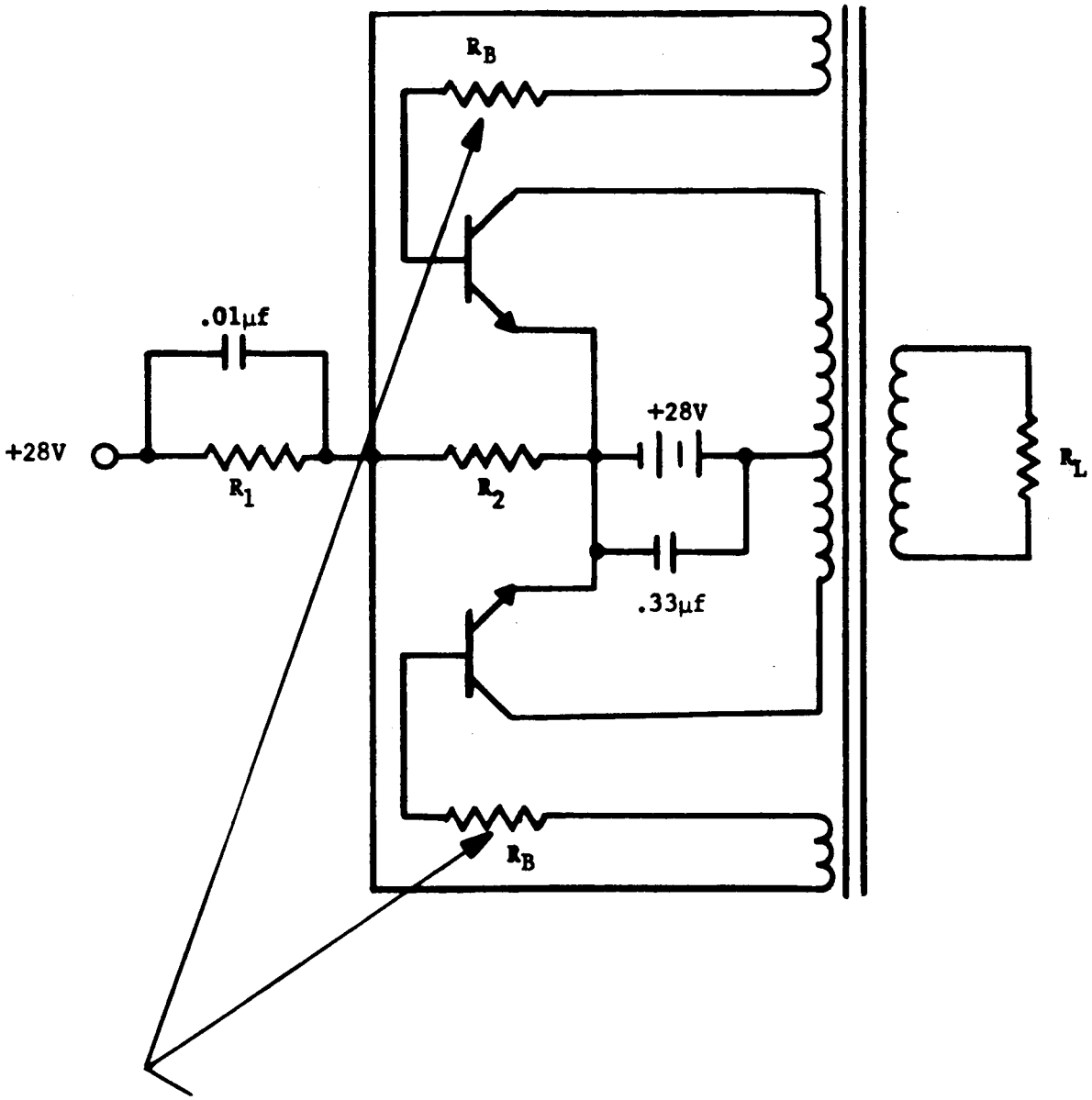
Efficiency Testing
Equipment

Figure 23



Close-up View
of Efficiency Test Setup

Figure 24



Resistors Inserted to Increase Efficiency in Emitter-Base Breakdown Mode of Operation

Figure 25

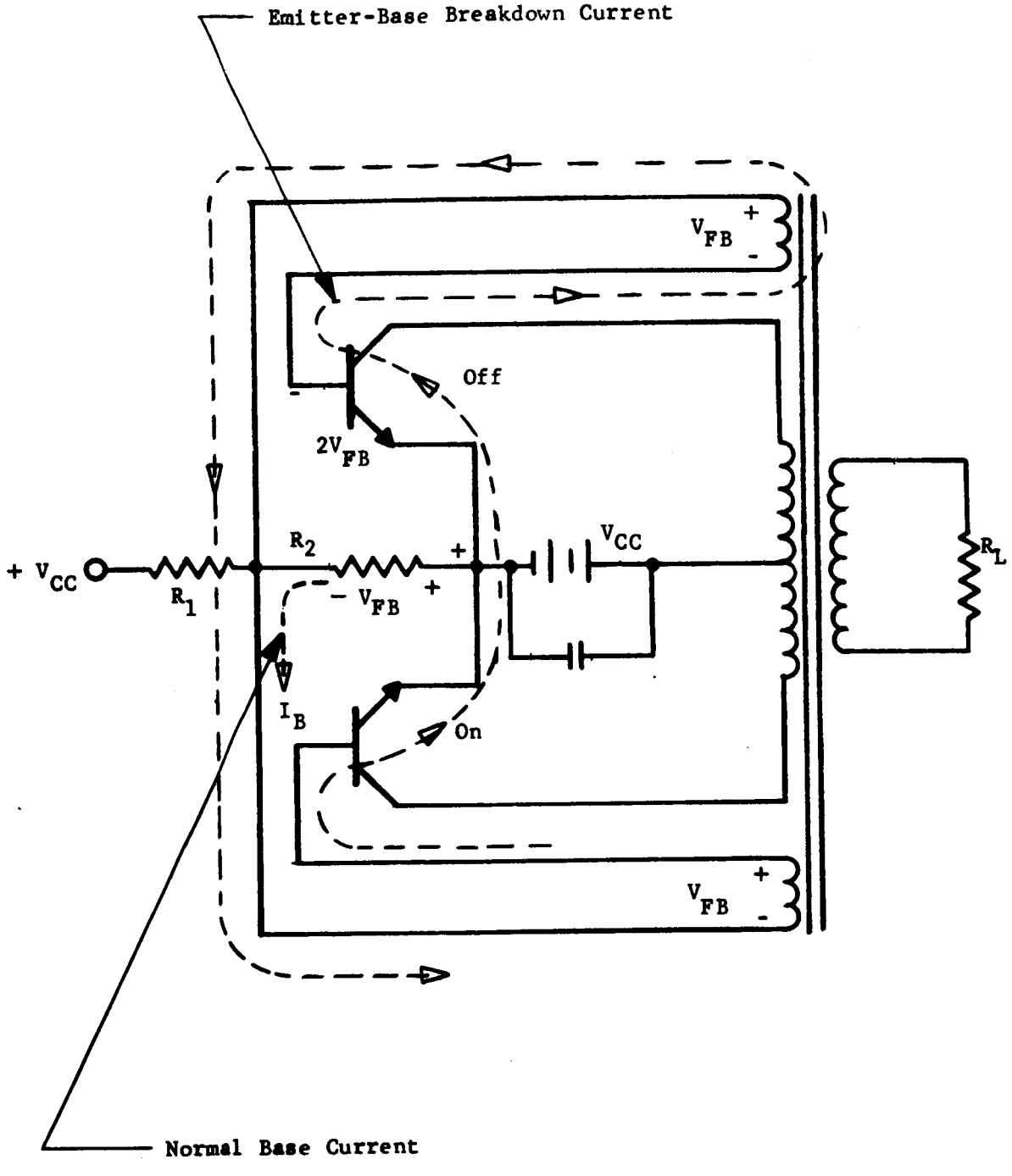


Figure 26: Circuit Diagram Showing Normal Voltages and Normal and Abnormal Base Currents

relationship is evident when voltage in the base loop of T_2 are summed in Figure 26.

The PIC units which were constructed had V_{EBO} voltages of approximately 7 volts. By reducing the number of feedback turns from 5 to 4 it was possible to eliminate the emitter base breakdown problem. Although in this case the feedback voltage is slightly greater than one half of V_{EBO}, the forward emitter-base voltage drop of the on transistor, and the slight increase in breakdown voltage above V_{EBO} due to reverse bias of the off transistor, allows proper circuit operation.

With the reduced amount of feedback voltage required to eliminate emitter-base breakdown, the parallel resistance of R_1 and R_2 must be reduced to obtain enough base current to switch the transistors properly.

R_1 and R_2 must, however, be kept in a certain ratio so the transistors will be slightly forward biased initially to allow oscillation to begin. Thus if R_2 is reduced to allow more base current to flow (as required by transistors with lower betas than those used in the original circuit) R_1 must also be reduced to retain the self starting property of the circuit. Lowering the values of R_1 and R_2 will result in greater power dissipation in the bias circuit, thus reducing the efficiency which can be expected. The method of calculating approximate bias resistor values follows.

Calculations (see Figure 27):

With essentially a square wave output, I_C (saturation collector current) can be found from:

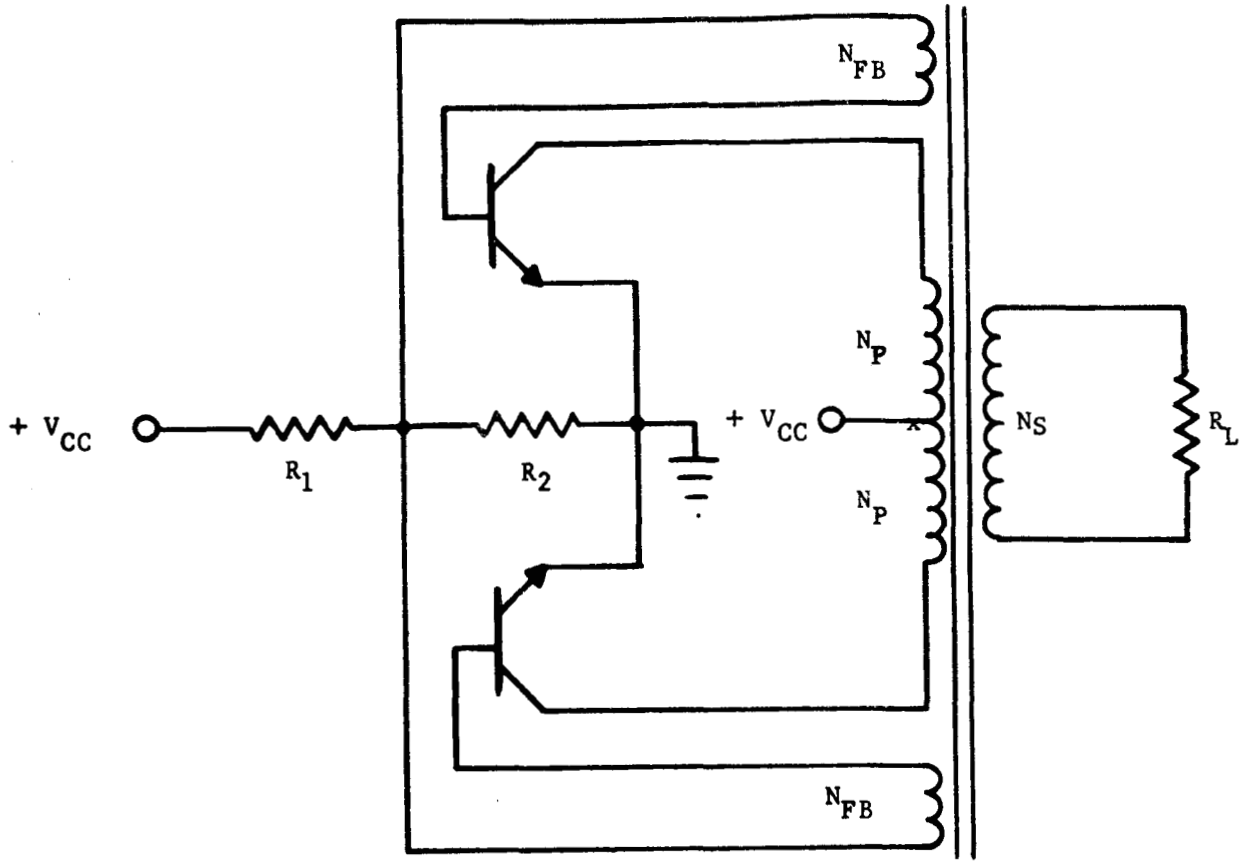
$$I_C = \frac{(V_{CC} - V_{CE(sat)})}{R_L} \quad \text{when } N_P = N_S.$$

Also I_B (saturation base current) is approximately

$$I_B = \frac{I_C}{\beta}.$$

I_B should actually be slightly higher than this value to assure saturation of the transistor.

Calculations for finding approximate bias resistor values for saturable core oscillators.



The following items are known:

V_{CC} - DC supply voltage

R_L - Load resistance

N_P - Turns on transformer primary

N_S - Turns on transformer secondary

V_{EBO} - Emitter-base breakdown voltage with collector open

$V_{EB(start)}$ - Voltage which initially forward biases transistors to allow self-starting.

$V_{EB(forward)}$ - Forward emitter-base voltage drop

$V_{CE(sat)}$ - Collector emitter saturation voltage

$\beta(h_{fe})$ - Current gain of transistors

Figure 27

The maximum feedback voltage is limited by the emitter base breakdown voltage

$$V_{FA(max)} = \frac{V_{EBO}}{2}$$

as evident from Figure 26.

Therefore the number of feedback turns needed can be determined.

$$N_{FB} = \frac{N_P \, V_{FB(max)}}{V_{CC} - V_{CE(sat)}}$$

The number of turns on the feedback coil must necessarily be an integer. This is due to the toroidal configuration of the transformer. If the calculated N_{FB} is just below some integral value, the slightly higher number of turns can usually be used. This is due to the forward emitter-base voltage which is present but not accounted for in the equation. Also there is somewhat of an increase in the emitter base breakdown voltage above V_{EBO} due to conditions in the oscillator circuit which are not apparent when V_{EBO} measurements are made with test equipment.

Once a value for N_{FB} is determined the actual amount of feedback voltage which will be generated on each feedback coil can be determined

$$V_{FB} = \frac{N_{FB} \, (V_{CC} - V_{CE(sat)})}{N_P}$$

The I_B value required for transistor saturation has been previously determined as:

$$I_B = \frac{I_C}{\beta}$$

plus some small amount of base current to insure saturation.

The next step is to determine the values of bias resistors which will allow proper base current to flow and also permit self starting.

A bias voltage $V_{EB(start)}$ must be selected to slightly forward bias both transistors; this is generally in the range of one volt.

We now have the two basic criteria for calculating bias resistor values, namely, I_B and $V_{EB(start)}$.

For proper starting bias,

$$V_{EB(start)} = \frac{R_2}{R_1 + R_2} V_{CC} .$$

To allow proper base current to flow

$$I_B = \frac{V_{FB} - V_{EB(forward)}}{R_1 R_2 / R_1 + R_2} .$$

Solving the equations for R_1

$$R_1 = \frac{V_{CC}(V_{FB} - V_{EB(forward)})}{I_B V_{EB(start)}}$$

and

$$R_2 = \frac{V_{CC}(V_{FB} - V_{EB(forward)})}{(V_{CC} - V_{EB(start)}) I_B} = \frac{R_1}{(\frac{V_{CC}}{V_{EB(start)}} - 1)}$$

$V_{EB(start)}$ was assumed to be approximately one volt, which simplifies the equations to

$$R_1 = \frac{V_{FB} V_{CC}}{I_B}$$

$$R_2 = \frac{R_1}{V_{CC} - 1} .$$

It should be realized that these equations are based on several approximations and will not necessarily provide best operation of the oscillator. They do however give values which will permit oscillation and thus provide a point from which to begin improving the operation.

D. f_t MEASUREMENTS

The transistors used in the PIC units were tested to obtain a value of f_t, the gain bandwidth product. This was done using the standard test setup used for all f_t measurements.

For the units tested, f_t was found to be approximately five megacycles. This should be adequate for circuit operation at 50kc. The frequency response of the transformer core affects switching time to a greater degree than do the transistors.

Figure 28 is a photograph of the equipment used for the f_t measurements.

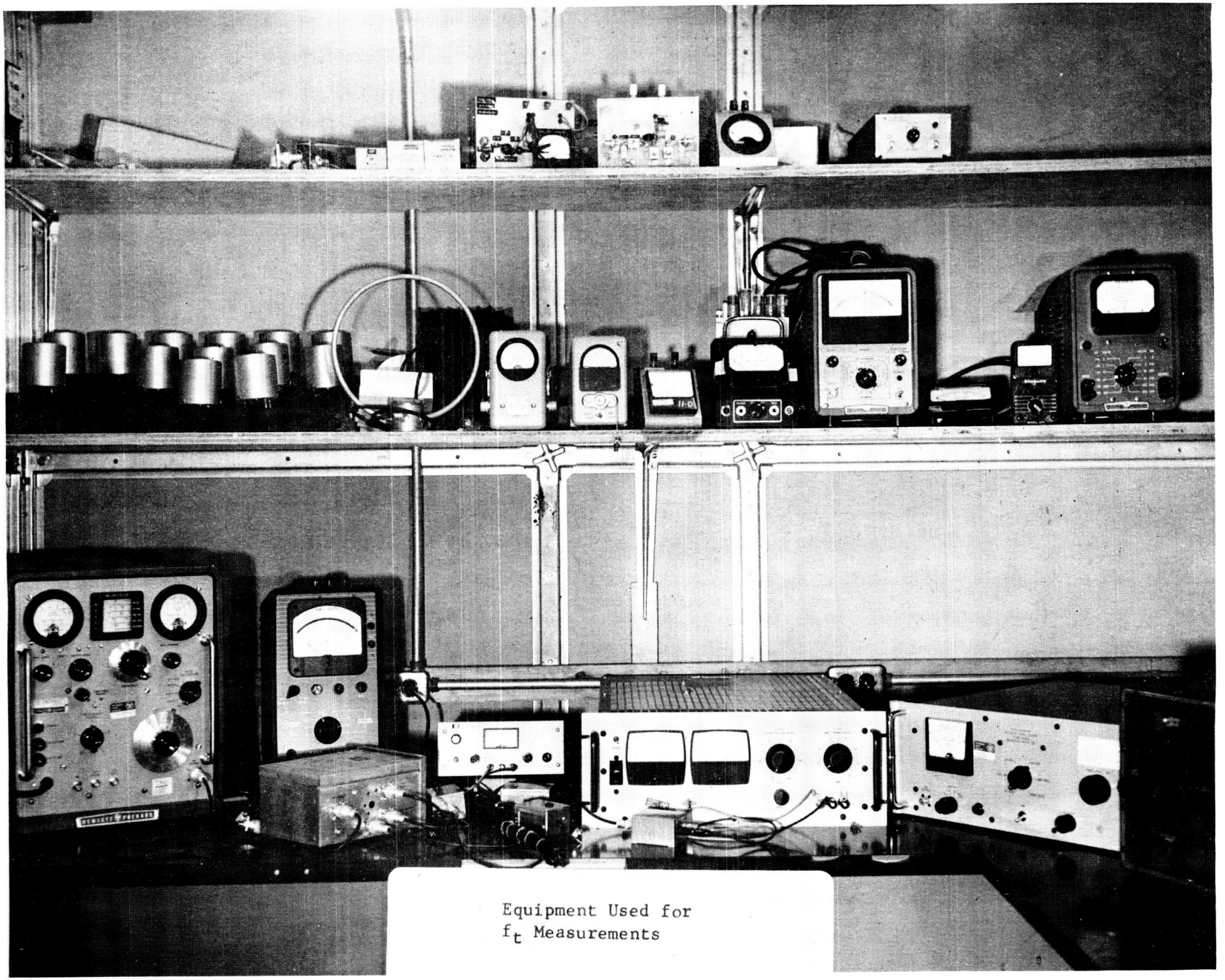
E. OSCILLATOR TESTS USING HIGH FREQUENCY DEVELOPMENTAL TRANSISTORS

Several Westinghouse HF-6 transistors were tried in the circuit to determine if greater switching capability would affect efficiency to any great extent. These transistors are experimental devices and have a gain bandwidth product of 150 megacycles. The betas were approximately 90. An efficiency of greater than 90% was obtained with the units. At the time the tests were run diodes were placed in the base leads to eliminate the reverse emitter-base breakdown problem. Greater efficiencies might have been obtained had the diodes not been necessary.

F. TESTING OF FINAL UNITS

The available resistor values in the PIC units did not permit optimum performance to be obtained from each unit. Several units which had low betas had no internal resistors of low enough value. Enough feedback current to maintain proper oscillation could not be obtained using internal resistors. External resistors were used to obtain proper oscillation and permit efficiency data to be taken.

On the low beta units it was considered desirable to use only one external resistor. One or two units are slow starting with the resistor values indicated. This is a result of the compromise of resistor values between necessary starting voltage and required base current.



Equipment Used for
f_t Measurements

Figure 28

Several of the units with relatively high betas exhibit good efficiencies. They are completely self-contained having no external resistors.

In all of these efficiency tests it was necessary to reduce the number of feedback turns. This eliminated the problem with reverse emitter base breakdown.

All but one of the units were tested with four feedback turns rather than the original five. One, however, due to its beta values and relatively low resistor values available internally could be operated with three feedback turns. The good efficiency obtained from this unit (#6) indicates that with less feedback required, efficiency increases.

G. SUMMARY OF TEST RESULTS AND RECOMMENDATIONS

1. High betas permit greater efficiencies in the suggested circuit configuration.

2. Collector emitter saturation and bias resistor losses seem to be the greatest factors affecting efficiency.

3. Greater efficiencies can possibly be obtained by circuit alterations which would decrease biasing and feedback losses.

4. The emitter-base reverse breakdown problem can be eliminated by reducing the amount of feedback voltage. This requires transistors of relatively high betas in order to keep starting bias losses to a minimum.

H. DATA ON INITIAL UNITS

Efficiency calculation formulas:

$$R_L = 33.5\Omega$$

$$P_{IN} = V_{IN} I_{IN}$$

$$P_{OUT} = \frac{V^2_{rms}}{R_L}$$

$$\text{Eff.} = \frac{100\ P_{OUT}}{P_{IN}}\ \% .$$

Definition of Symbols

V_{CC} = DC supply voltage

R_L = Load resistance

N_P = Turns on transformer primary

N_S = Turns on transformer secondary

N_{FB} = Turns on transformer feedback coil

V_{EBO} = Emitter base breakdown voltage with collector open

$V_{EB(start)}$ = Voltage which initially forward biases transistors to allow self starting of oscillator

$V_{EB(forward)}$ Forward emitter-base voltage drop

$V_{CE(sat)}$ = collector emitter saturation voltage

β (h_{fe}) = current gain of transistor

f_t = gain bandwidth product

I_C = collector current

I_B = base current

R_1 = large bias resistor

R_2 = small bias resistor

PIC = Power Integrated Circuit

Data From Initial Efficiency Testing

	V_{IN}	I_{IN}	P_{IN}	V_{OUT} rms	P_O	I_B ma	Eff.	Snap In V
Unit No. 131								
R_B = 0Ω	28	.86	24.1	25.4	19.25	400	80	27.8
R_B = 1.35	29	.855	24.8	26.25	20.55	300	83	29
R_B = 2.7	30	.87	26.1	27.15	22	300	84.3	30
Unit No. 241								
R_B = 0Ω	77	.92	24.85	25.8	19.88	400	80	26
R_B = 2.7	28	.875	24.5	26.9	21.6	200	88	27
R_B = 1.35	28	.915	25.6	26.8	21.4		83.6	26.5
Unit No. 251								
R_B = 27Ω	30	.875	26.27	27.3	22.25	260	84.6	30
R_B = 1.35	29	.85	24.6	26.3	20.65	270	84	28.8
R_B = 0	29	.92	26.7	26	20.2	480	75.6	28.8
Unit No. 261								
R_B = 1.35	29	.855	24.8	26.25	20.6	170	83	28.8
R_B = 0	28	.85	23.8	25.2	18.95	460	79.6	28
R_B = 2.7	30	.87	26.1	27.3	22.25	280	85.2	29.5
Unit No. 271								
R_B = 0	28	.932	26.1	25.3	19.1	400	73.3	27.7
R_B = 1.35	28	.82	22.95	25.4	19.25		84	
R_B = 2.7	28.25	.805	22.75	25.75	19.8	160	87	

Parameters of Oscillator Units Used in Initial Efficiency Tests

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{FE}	V_{CE} sat.	I_C				
131	100	.1	100	.4	7	.01	8	.5	R_1R_2	R_1R_3	R_2R_3	R_2R_5	R_3R_5
	100	1.	100	1.	7	.01	8	.5	1850	4000	5250	4600	435
241	90	12.	90	12.	7	15.	20	.35	R_1R_2	R_1R_4	R_1R_6	R_2R_4	R_4R_6
	90	1.	90	1	7	.01	20	.45	1550	4200	4500	2500	450
251	90	.02	90	.01	7	.01	8	.5					
	100	.5	90	.3	7	.01	15	1.	2200	5400	6000	3300	510
261	90	1.	90	1.	7	.01	8	.5					
	80	.4	80	.5	7	.01	12	.6	1800	4900	500	2900	4200
271	90	2.0	9	2.	7	.01	15	.6					
	90	.2	80	.2	7	.01	25	.6	1920	5000	3500	3000	480

I. DATA ON OSCILLATOR CIRCUIT USING HF-6 TRANSISTORS

1. Units 49 and 53

R_2 = 390Ω//300

R_1 = 4.7K//4.7K

V_{IN} = 28

I_{IN} = .92

P_{IN} = 25.75

V_O = 27.7

P_O = 22.9

V_{CE} = ~.3

V_B --> .35 --> .8

N_{FB} = 5

Snap in ~17V Eff. = 89%

Diodes in base lead to prevent E-B breakdown.

2. Units 49 and 53

R_2 = 390Ω//800

R_1 = 4.7K//4.7K

V_{IN} = 28

I_{IN} = .88

P_{IN} = 24.65

V_O = 27.7

P_O = 22.9

N_{FB} = 5

Snap in ~28V Eff. = 92.8%

Parameters of HF-6 Transistors

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{FE}	I_C	sat.	I_C	I_B
49	120	10	110	10	6	< 1	90	1A	2.7V	5A	.3A
53	510	10	130	10	6	< 1	91	1A	0.8V	5A	.3A

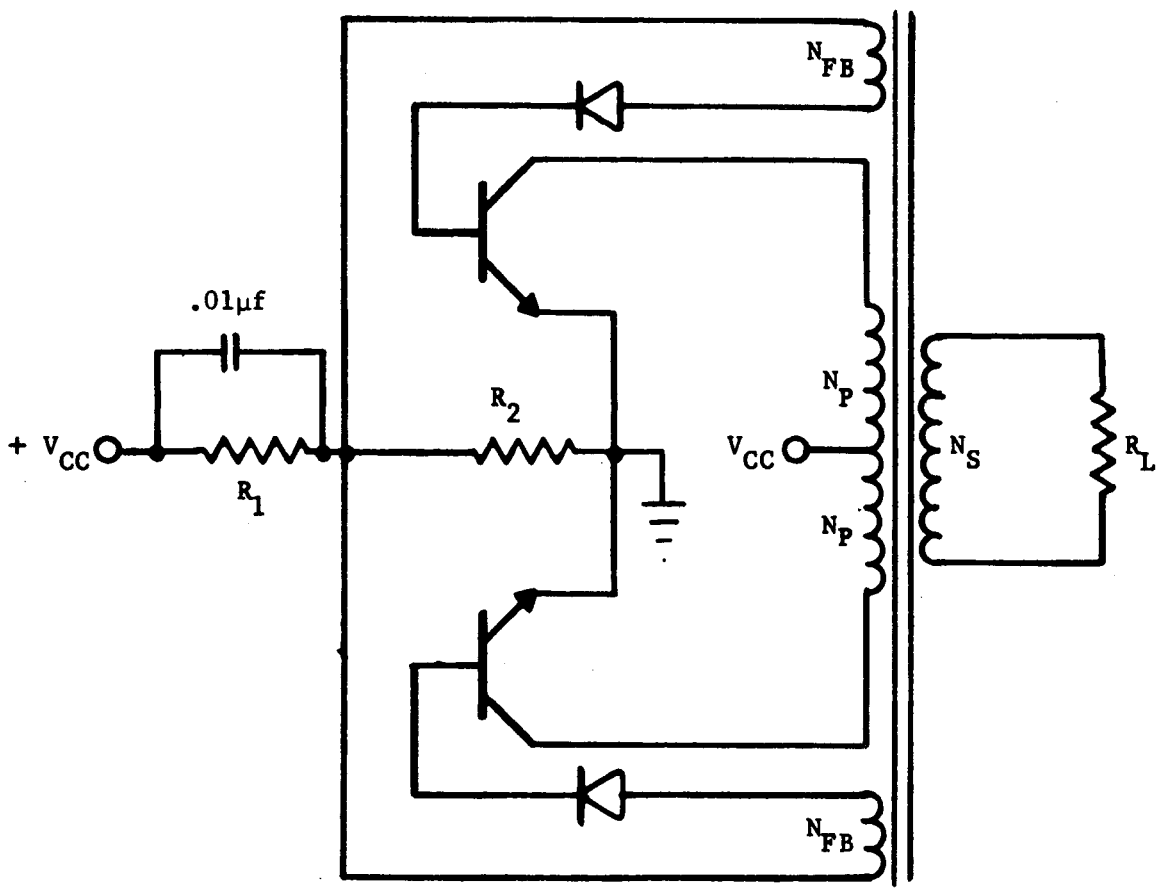


Figure 29: Circuit Diagram for Efficiency Tests Using HF-6 Transistors

J. CALCULATIONS ON FINAL UNITS

$R_L = 34.5\Omega$

$P_{IN} = V_{IN}I_{IN}$

$P_{OUT} = \frac{V_o^2}{R_L}$

$Eff. = \frac{P_{OUT} \times 100\%}{P_{IN}}$

Bias resistor values shown for each individual unit.

Pin connections listed for each unit.

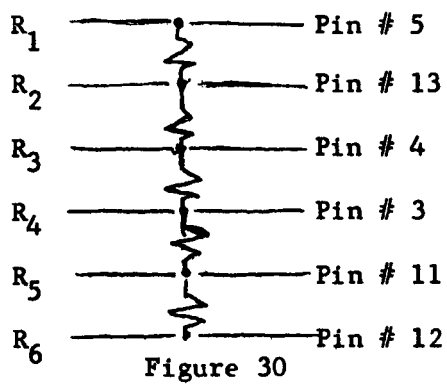


Figure 30

Integrated oscillator test unit #4.

$R_1' = R_1R_2//R_2R_3//R_3R_4 = 990\Omega$

$R_2' = R_4R_5//R_5R_6 = 217\Omega$

$N_{FB} = 4$ turns

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	GR
4	+28	12	D-J
5	+28	13	D-J
6	Open	14	Open
7	I	15	GR
8	H	16	GR

Oscillates at 31VDC supply voltage.

V_{IN} = 31VDC

I_{IN} = .83A

P_{IN} = 25.72

V_{OUT} = 28V rms

P_{OUT} = 22.72

N_{FB} = 4 turns

R_L = 34.5Ω

Eff. = 88.5%

Integrated oscillator test unit #6.

$R_1' = R_3R_4 = 1.65K$

$R_2' = R_4R_5//R_5R_6 = 153\Omega$

N_{FB} = 3 turns

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	GR
4	+28	12	D-J
5	Open	13	Open
6	Open	14	Open
7	I	15	GR
8	H	16	GR

with N_{FB} = 3 turns.

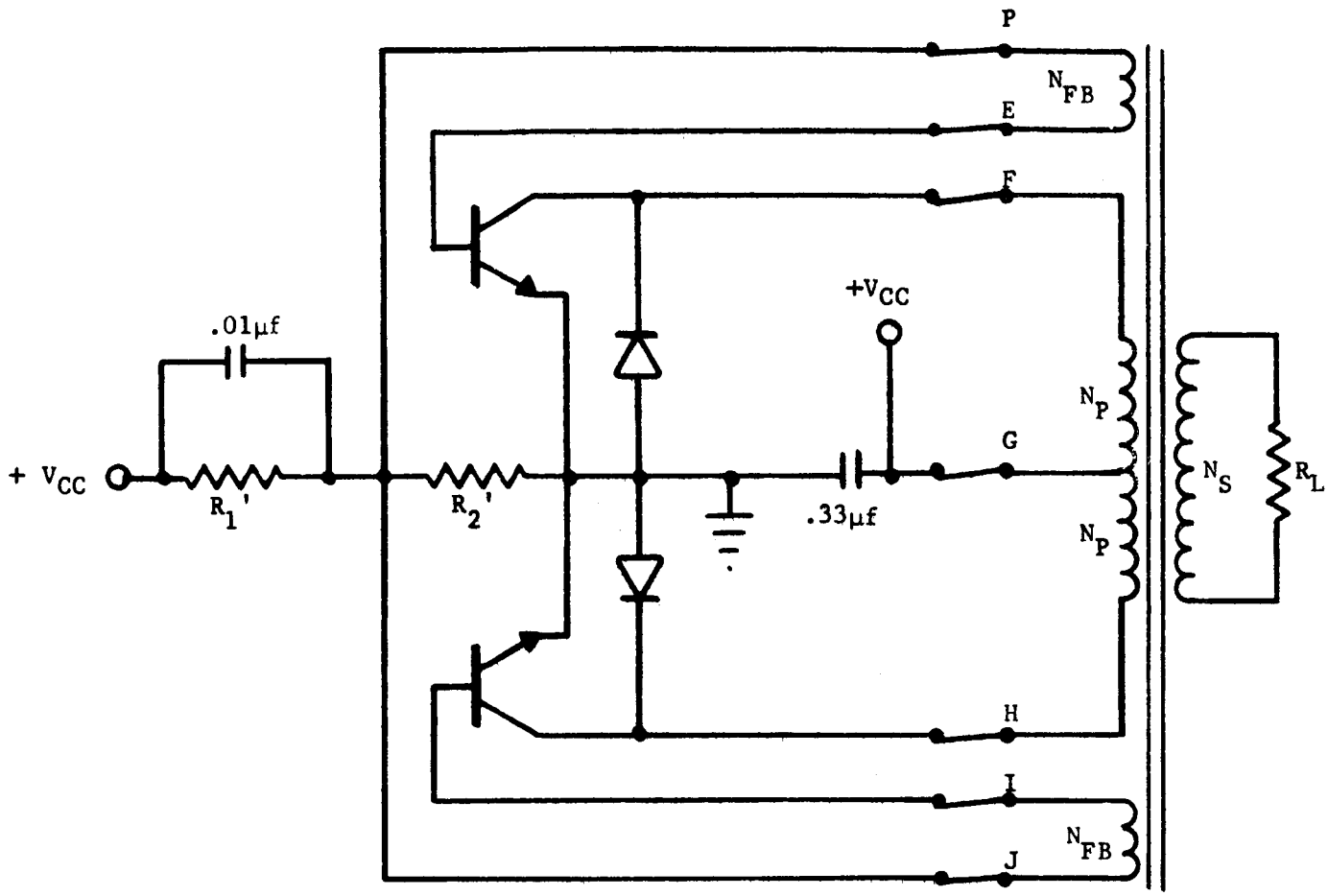
V_{IN} = 28V

I_{IN} = .8A $\quad P_{OUT}$ = 20.9

P_{IN} = 22.4 $\quad R_0$ = 34.5Ω

V_{OUT} = 26.85V rms $\quad$ Eff. = 94%

Circuit Used to Test the Final Units



N_P = 29 N_S = 29 N_{FB} = See individual sheets

Transformer core, magnetics #80586 - 1/4D Permaloy 80

Pin Placement

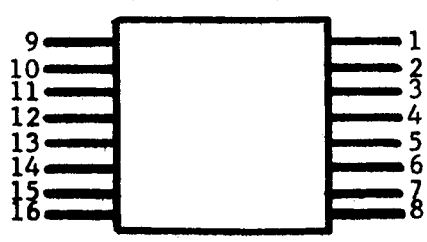


Figure 31

Integrated oscillator test unit #8.

Calculation of approximate bias resistor values.

$$R_1' = \frac{V_{CE}\, V_{EB}}{I_B} = \frac{28.3}{.8/12.5} \doteq 1.3K$$

$$R_2' = \frac{R_{7.5K}}{V_{cc}-1} = \frac{1.3K}{27} = 48.6\Omega$$

$V_{IN} = 28$

$I_{IN} = .78$

$P_{IN} = 21.8$

$V_{OUT} = 25.0$

$P_{OUT} = 18.1$

$R_1' = R_4 R_6 \doteq 1K$

$R_2' = 56\Omega$ external

Eff. = 83%

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	+28	11	Open
4	Open	12	D-J
5	Open	13	Open
6	Open	14	Open
7	I	15	GR
8	H	16	GR

56Ω external from D-J to ground.

Integrated oscillator test unit #9.

Calculation of approximate bias resistor values.

$$R_1' = \frac{V_{CC}\ V_{EB}}{I_B} = \frac{28.3}{.8/11} = 1.15K$$

$$R_2' = \frac{R_{7.5K}}{V_{CC} - 1} = \frac{1.15K}{27} = 39.8\Omega$$

V_{IN} = 28

I_{IN} = .745

P_{IN} = 20.85

V_{OUT} = 24.9

P_{OUT} = 18.0

R_1 = $R_1R_2//R_3R_4$ = 1.44K

R_2 = 47Ω external

N_{FB} = 4 turns

Pin connection same as unit #11

47Ω resistor from D-J to ground.

Eff. = 86.2

Integrated oscillator test unit #10.

Calculation of approximate bias resistor values.

$$R_1' = \frac{V_{CC}\ V_{FB}}{I_B} = \frac{28.3}{.8/13} = 1.37K$$

$$R_2' = \frac{R_{7.5K}}{V_{CC} - 1} = \frac{1.37K}{27} = 50.6\Omega$$

V_{IN} = 28A

I_{IN} = .78A

P_{IN} = 21.8

V_{OUT} = 25.75 rms

P_{OUT} = 19.2

R_1' = $R_1R_2//R_3R_4$ = 1.39K

R_2' = 47Ω external

N_{FB} = 4 turns

Eff. = 88.1%

Pin connection same as unit #11.

47Ω resistor from D-J to ground.

Integrated oscillator test unit #11.

Calculation of approximate bias resistor values.

$$R_1' = \frac{V_{CC}\ V_{FB}}{I_B} = \frac{28.3}{.8/16.7} = \frac{84}{.048m} = 1.75K$$

$$R_2' = \frac{R_{7.5K}}{V_{CC} - 1} = \frac{1.75K}{27} = 65\Omega$$

V_{IN} = 28

I_{IN} = .76

P_{IN} = 21.3

V_{OUT} = 25.5

P_{OUT} = 18.85

R_1 = 1.5K ($R_1R_2//R_3R_4$)

R_2 = 56Ω external

N_{FB} = 4 turns

Eff. = 88.5%

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	Open
4	+28	12	Open
5	D-J	13	+28
6	Open	14	Open
7	I	15	GR
8	H	16	GR

External 56Ω resistor from D-J to ground.

Integrated oscillator test unit #13.

$R_1' = R_1R_3 = 5K$

$R_2' = R_5R_6 = 430\Omega$

$N_{FB} = 4$ turns

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	Open	11	D-J
4	D-J	12	GR
5	+28	13	Open
6	Open	14	Open
7	I	15	GR
8	H	16	GR

$V_{IN} = 28V$

$I_{IN} = .8A$

$P_{IN} = 22.4$

$V_{OUT} = 27V$ rms

$P_{OUT} = 21.6$

$R_L = 34.5\Omega$

Eff. = 94.4%

Integrated oscillator test unit #26.

Calculation of approximate bias resistor values.

$$R_1' = \frac{V_{CC}\ V_{FB}}{I_B} = \frac{28.3}{.8/8} = 933\Omega$$

$$R_2' = \frac{R_{7.5K}}{V_{CC}-1} = \frac{933}{27} = 34.6\Omega$$

Let $R_1' = R_1R_2//R_2R_4 \doteq 1.11K$

R_2 = 42Ω external

V_{IN} = 30

I_{IN} = .8

P_{IN} = 24.0W

V_{OUT} = 27.3

P_{OUT} = 21.6

Eff. = 90%

N_{FB} = 4 turns

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	Open
4	Open	12	Open
5	D-J	13	+28
6	Open	14	Open
7	I	15	GR
8	H	16	GR

Integrated oscillator test unit #31.

Similar low β to unit #26.

So approximate values

$R_1' = 933\Omega$

$R_2' = 34.6\Omega$

Let $R_1' = R_1R_2//R_2R_4 = 1.17K\ \Omega$

$R_2' = 45\Omega$

$V_{IN} = 30$

$I_{IN} = .79$

$P_{IN} = 23.7$

$V_{OUT} = 26.7$

$P_{OUT} = 20.65$

$N_{FB} = 4$ turns

Eff.= 87%

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	Open
4	Open	12	Open
5	D-J	13	+28
6	Open	14	Open
7	I	15	GR
8	H	16	GR

PIC Unit #52

Pin No.	To	Pin No.	To
1	F	9	GR
2	E	10	GR
3	D-J	11	GR
4	D-J	12	D-J
5	D-J	13	+28
6	Open	14	Open
7	I	15	GR
8	H	16	GR

$R_1' = R_1R_2//R_2R_3 \doteq 1.3K$

$R_2' = R_4R_5//R_5R_6 = 133\Omega$

$V_{IN} = 28VDC$

$P_{IN} = 22.96W$

$V_{OUT} = 26.6Vrms$

$P_{OUT} = \frac{(26.6)^2}{34.5} = 20.5W$

$R_{LOAD} = 34.5\Omega$

$N_{FB} = 4$ turns

$I_{IN} = .82ADC$

Eff. = 89.4%

Table II

LEAD CONFIGURATION
OF FINAL UNITS

PIN NO.	CONNECTION
1	$Collector_2$
2	$Base_2$
3	R_4
4	R_3
5	R_1
6	Blank
7	$Base_1$
8	$Collector_1$
9	Emitter
10	Emitter
11	R_5
12	R_6
13	R_2
14	Blank
15	Emitter
16	Emitter

Table III

ELECTRICAL PARAMETERS
OF FINAL UNITS

UNIT NO.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} .5a	h_{fe} 1a	Efficiency % at 20 watts	N_{FB} No. turns
8	100	15	100	20	7	.8	12.5	11	83	4
	100	15	100	20	7	.1	33	38.4		
9	100	15	100	20	7	1.5	12.5	13.2	86.2	4
	100	6	100	10	7	1.2	11.5	11.3		
10	100	10	100	10	6	3.5	13	13.5	88.1	4
	100	10	100	12	7	1	14.7	15.2		
11	100	10	100	10	7	.01	16.7	17.6	88.5	
	100	4	100	5	7	.02	16.7	15.6		
23	90	1	90	1	7	.01	12	12.5	90	4
	80	.4	80	.5	7	.01	14	15		
31	100	10	90	10	7	.01	16	16.5	87	4
	100	6	90	10	7	.01	7	9		

Table IV

ELECTRICAL PARAMETERS
OF FINAL UNITS

UNIT NO.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} .5a	h_{fe} .1a	Efficiency % at 20 watts	N_{FB} No. turns
4	100	2	100	2.5	7	.01	23.8	24.4	88.5	4
	100	1	100	1	7	.05	25	31		
6	100	10	90	20	7	.01	45	45.5	94	3
	95	10	80	20	7	.01	45	45.5		
13	100	30	70	20	7	.01	100	100	94.4	4
	100	30	75	20	7	.01	100	100		
52	100	5	100	5	7	.01	30	30	89.4	4
	100	1	100	2	7	.01	30	30		

Table V

TYPICAL RESISTOR VALUES
FOR FINAL UNITS

UNIT NO.	R_1 R_2	R_1 R_4	R_1 R_6	R_2 R_4	R_2 R_6	R_3 R_4	R_4 R_5	R_4 R_6	R_5 R_6
	-- Resistor Taps in ohms								
4	3,250	9,300	11,000	6,000	8,000	2,300	340	940	600
6	2,300	-	-	-	-	-	220	720	500
13	3,250	6,750	7,000	4,250	5,000	-	240	670	430
52	2,200	9,500	11,000	9,000	10,000	-	200	600	400
8	-	-	-	-	-	2,500	360	1,000	650
9	3,600	10,000	11,000	6,000	7,000	2,400	340	950	610
10	3,500	8,000	11,000	5,500	6,000	2,300	330	930	600
11	4,000	10,000	11,000	6,000	8,000	2,400	470	1,100	650
26	1,700	4,400	5,000	-	3,250	-	410	-	-
31	-	4,500	5,000	2,800	3,250	-	400	-	-

V. CONCLUSIONS AND RECOMMENDATIONS

The feasibility of monolithic power integrated circuitry has been demonstrated. The major difficulties have been resolved. Optimization of the oscillator block or a comparable device toward any specific application can now be achieved with only minor modifications.

It is recommended that the techniques developed for this contract be considered for integrating power devices of similar nature in improving the space, weight and reliability requirements of equipment or systems.